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Home

Editorial

SECTION-II
(ADVANCED RESEARCH IN MECHANICAL ENGINEERING)

Editorial

The new economic millennium is surprisingly rushing with Innovation and Technology. There is a sharper focus on deriving value from the widespread global integration in almost all spheres of social, economic, political and technological subsystems. In the quest of making this earth a better place to live we have to make a strong hold upon sustainable energy source. Sustainable energy sources include all renewable energy sources, such as hydroelectricity, solar energy, wind energy, wave power, geothermal energy, bioenergy, and tidal power. It usually also includes technologies designed to improve energy efficiency. Energy efficiency and renewable energy are said to be the twin pillars of sustainable energy. Renewable energy technologies are essential contributors to sustainable energy as they generally contribute to world energy security, reducing dependence on fossil fuel resources, and providing opportunities for mitigating greenhouse gases. Although the discipline like electrical engineering has narrated academic maturity in the last decades, but the limitations of the non renewable energy sources, turbulence and disturbances in the energy propagation cascades various insightfulness and stimulation in post classical electrical era. Evidence shows that there are phenomenal supplements in power generation and control after the introduction of Energy Management System (EMS) supported by Supervisory Control and Data Acquisition (SCADA). As there is increasing focus on strengthening the capacity of the power houses with the existing resources or constraints some new dimensions like FACTS, Optimal System Generation, High Voltage DC transmission system, Power Generation Control, Soft Computing, Compensation of transmission line, Protection scheme of generator, Loss calculation, economics of generation, fault analysis in power systems are emerging. Since the world is suffering with water, food, and energy crisis, energy consumption has social relevancy.

Let me highlight some of the recent developments in Electronics discipline. The new integrated devices did not find a ready market. Users were concerned because the individual transistors, resistors, and other electronic circuit components could not be tested individually to ensure their reliability. Also, early integrated circuits were expensive, and they impinged on the turf that traditionally belonged to the circuit designers at the customer's company. Again, Bob Noyce made a seminal contribution. He offered to sell the complete circuits for less than the customer could purchase individual components to build them. (It was also significantly less than it was costing us to build them!) This step opened the market and helped develop the manufacturing volumes necessary to reduce manufacturing costs to competitive levels. To this day the cost reductions resulting from economies of scale and newer high-density technology are passed on to the user—often before they are actually realized by the circuit manufacturer. As a result, we all know that the high-performance electronic gadget of today will be replaced with one of higher performance and lower cost tomorrow.

The integrated circuit completely changed the economics of electronics. Initially we looked forward to the time when an individual transistor might sell for a dollar. Today that dollar can buy tens of millions of transistors as part of a complex circuit. This cost reduction has made the technology ubiquitous—nearly any application that processes information today can be done most economically electronically. No other technology that I can identify has undergone such a dramatic decrease in cost, let alone the improved performance that comes from making things smaller and smaller. The technology has advanced so fast that I am amazed we can design and manufacture the products in common use today. It is a classic case of lifting

ourselves up by our bootstraps—only with today's increasingly powerful computers can we design tomorrow's chips.

In the advent of modern research there is a significant growth in Mechanical Engineering as Computer Aided Design has become instrumental in many industrialized nations like USA, European Countries, Scotland and Germ Other CAE programs commonly used by mechanical engineers include product lifecycle management (PLM) tools and analysis tools used to perform complex simulations. Analysis tools may be used to predict product response to expected loads, including fatigue life and manufacturability. These tools include Finite Element Analysis (FEA), Computational Fluid Dynamics (CFD), and Computer-Aided Manufacturing (CAM). Using CAE programs, a mechanical design team can quickly and cheaply iterates the design process to develop a product that better meets cost, performance, and other constraints. No physical prototype need be created until the design nears completion, allowing hundreds or thousands of designs to be evaluated, instead of a relative few. In addition, CAE analysis programs can model complicated physical phenomena which cannot be solved by hand, such as viscoelasticity, complex contact between mating parts, or non-Newtonian flows.

As mechanical engineering begins to merge with other disciplines, as seen in mechatronics, multidisciplinary design optimization (MDO) is being used with other CAE programs to automate and improve the iterative design process. MDO tools wrap around existing CAE processes, allowing product evaluation to continue even after the analyst goes home for the day. They also utilize sophisticated optimization algorithms to more intelligently explore possible designs, often finding better, innovative solutions to difficult multidisciplinary design problems.

Apart from Industrial Development there is also an hourly need for creation of an influential professional body which can cater to the need of research and academic community. The current scenario says there exists a handfull of bodies like American Society of Mechanical Engineers (ASME). Hence we must strive towards formation of a harmonious professional research forum committed towards discipline of Mechanical Engineering.

In the current scenario of scientific development robotics takes a center stage in solving many social problems. As agriculture is the mainstay of many developing nations, efficiency building measures should be incorporated in the field to boost efficiency and productivity. In the context Robotics in agriculture has attracted much attention in the recent years. The idea of robotic agriculture (agricultural environments serviced by smart machines) is not a new one. Many engineers have developed driverless tractors in the past but they have not been successful as they did not have the ability to embrace the complexity of the real world. Most of them assumed an industrial style of farming where everything was known before hand and the machines could work entirely in predefined ways – much like a production line. The approach is now to develop smarter machines that are intelligent enough to work in an unmodified or semi natural environment. These machines do not have to be intelligent in the way we see people as intelligent but must exhibit sensible behavior in recognized contexts. In this way they should have enough intelligence embedded within them to behave sensibly for long periods of time, unattended, in a semi-natural environment, whilst carrying out a useful task. One way of understanding the complexity has been to identify what people do in certain situations and decompose the actions into machine control.

The use of MATLAB is actually increasing in a large number of fields, by combining with other toolboxes, e.g., optimization toolbox, identification toolbox, and others. The Math Works Inc. periodically updates MATLAB and Simulink, providing more and more advanced software. MATLAB handles numerical calculations and high-quality graphics, provides a

convenient interface to built-in state-of-the-art subroutine libraries, and incorporates a high-level programming language. Nowadays, the MATLAB/Simulink package is the world's leading mathematical computing software for engineers and scientists in industry and education.

Due to the large number of models and/or toolboxes, there is still some work or coordination to be done to ensure compatibility between the available tools. Inputs and outputs of different models are to-date defined by each modeler, a connection between models from two different toolboxes can thus take some time. This should be normalized in the future in order to allow a fast integration of new models from other toolboxes. The widespread use of these tools is reflected by ever-increasing number of books based on the Math Works Inc. products, with theory, real-world examples, and exercises.

The conference is designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these two integrated disciplines. Even a fraction of active participation deeply influences the magnanimity of this international event. I must acknowledge your response to this conference. I ought to convey that this conference is only a little step towards knowledge, network and relationship

I express best wishes to all the paper presenters. I extend my heart full thanks to the reviewers, editorial board members, programme committee members of the conference. If situations prevail in favor we will take the glory of organizing the second conference of this kind during this period next year.

Convenor

Bikash Chandra Rout
Technical Editor, IOAJ

SECTION –I
(ELECTRICAL ENGINEERING AND COMPUTER SCIENCE)

DESIGN AND ANALYSIS OF LLC RESONANT CONVERTER FOR DRIVING HIGH POWER LEDS

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Abstract— This paper proposes a design and analysis of LLC resonant converter for high power LED driver .The presented circuit mainly consists of LLC resonant converter. This LLC resonant converter is designed for obtaining soft-switching on power switches and also to reduce their switching losses. The proposed driver controls the brightness of the LED lightening through dimming technique.Here dimming is mainly achieved through by varying the potentiometer on the driver circuit. Microcontroller with relays provides an option for selecting two output voltages from the LLC resonant converter to drive the high power LEDs. The proposed driver features cost-effectiveness, low levels of input current ripple, low switching losses, fewer components and reduced leakage current. Finally, a prototype driver developed to supply high-power LEDs with utility-line input voltage.

Keyword*:* Converter, LED driver, LLC resonant converter,

1. INTRODUCTION

Although in existence for many years, only recently has the LLC resonant converter, in particular in its half-bridge implementation, gained in the popularity it certainly deserves. In many applications, such as flat panel TVs, 85+ ATX PCs or small form factor PCs, where the requirements on efficiency and power density of their SMPS are getting tougher and tougher, the LLC resonant half-bridge with its many benefits and very few drawbacks is an excellent solution." In fact the introduction of new regulations, both voluntary and mandatory, has brought about a revaluation of the LLC series resonant topology. In LED lighting, to name just one of the infinite applications, the need for more and more efficient power supply systems is pushing power designers in this direction. All the main manufacturers of active components currently available on the SMPS market have included efficient chips in their product catalogues. With an effectively contained degree of circuit complexity, they allow the realization of power supplies with 90-96% efficiency, (which can be improved further using synchronous rectifiers instead of output diodes) and reduced EMI/EMC problems in comparison to other topologies. Generally speaking, resonant converters are switching converters that include a tank circuit actively participating in determining input-to-output power flow.The operating principle is based on the characteristic gain curve of the resonant tank, which allows to change the gain by a moderate variation of the switching frequency, thus resulting in an effective regulation of output voltage or current in relation to load and input voltage changes. The resonant tank is a set of two inductive elements and one capacitor (LLC).Even if the use of three different components, i.e. a discrete inductor, a conventional transformer and a capacitor is technically possible. Recently, light-emitting diodes (LEDs) have become increasingly popular as solid-state lighting sources. They differ from traditional incandescent lamps, which use filaments to make heat radiation, and fluorescent lamps, which use gaseous discharging. LEDs, which encompass almost all visible light and color, have features of compact
size, fast response and long lamp life. LEDs have many superior characteristics and effective applications in background lighting, displays, street lighting, automotive lighting, decorative lighting, and so on. Because of their long life and low maintenance costs, and they have been the main trend in modern lighting. The lighting applications of LEDs in our daily lives are closely related. The conventional LED driver is a two-stage topology, as shown in Fig. 1. The commonly used first stage is the boost converter, and the second stage is the half-bridge-type series resonant converter (SRC). The advantages of the first stage in the traditional driver are: (a) simple structure; (b) the input inductor can suppress the surging input current; (c) the power switch is non-floating, so it's easy to design the driver circuit. In addition, the inductor current equals the output current. Thus, it's easy to realize current-mode control. However, the output voltage is high, and the voltage stresses of the diode and the power switches are relatively high. For the second stage in the conventional driver, two symmetrically operated power switches, *S2* and *S3,* are series connected to form a half-bridge-type network. Their duty cycles are 50% and do not overlap while the two switches turn on or turn off. The resonant tank is composed of an inductor *Lr*, a capacitor *Cr* and a center-tapped transformer *T1*. The center-tapped transformer is connected with two diodes for full-wave rectifications, and the transformer is capable of providing low voltage and high current sources from the half bridge resonant

tank. The resonant inductor *Lr* and capacitor *Cr* dominate the resonant frequency of the SRC for achieving zero-voltage switching (ZVS) or not. A load that is too light causes low resonant current. Thus, the intrinsic capacitor of the power switch can not fully discharge energy; ZVS is unable to be achieved [2].

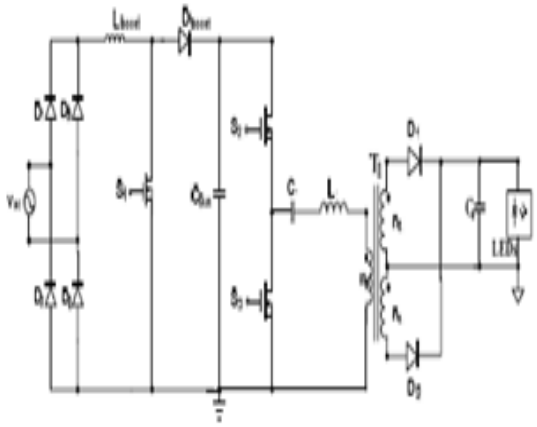

Figure 1. The Conventional two stage driver for LEDs.

II. THE PROPOSED LLC RESONANT CONVERTER FOR HIGH POWER LED DRIVER

Fig 2 presents the proposed high power LED driver which mainly works with utility input voltage of 230V.bridge rectifier is an arrangement of four (or more) diodes in a bridge circuit configuration that provides the same polarity of output for either polarity of input. When used in its most common application, for conversion of an alternating current (AC) input into a direct current (DC) output, it is known as a bridge rectifier. A bridge rectifier provides full-wave rectification from a two-wire AC input. For many applications, especially with single phase AC where the full-wave bridge serves to convert an AC input into a DC output, the addition of a filter capacitor may be desired because the bridge alone supplies an output of pulsed DC. The function of this capacitor, known as a reservoir capacitor (or smoothing capacitor) is to lessen the variation in (or 'smooth') the rectified AC output voltage waveform from the bridge. There is still some variation, known as "ripple". One explanation of 'smoothing' is that the capacitor provides a low impedance path to the AC component of the output, reducing the AC voltage across, and AC current through, the resistive load. In less technical terms, any drop in the output voltage and current of the bridge tends to be canceled by loss of charge in the capacitor. This charge flows out as additional current through the load. Thus the change of load current and voltage is reduced relative to what would occur without the capacitor. Increases of voltage correspondingly store excess charge in the capacitor, thus moderating the change in output voltage / current. The switching circuit mainly consists of LLC resonant converter.LLC resonant converter consists of LLC resonant tank which mainly consists of set of two inductive elements and one capacitor is designed by using discreet inductor, conventional transformer and capacitor. which provides the soft switching on power switch and reduces the switching losses. Relay selection mainly consists of relays. relay is an electrically operated switch. Most of the relays use an electromagnet to perform the switching operation mechanically but other operating principles are also used. Relays are components which allow a low-power circuit to switch a relatively high current on and off or to control signals that must be electrically isolated from the controlling circuit itself.

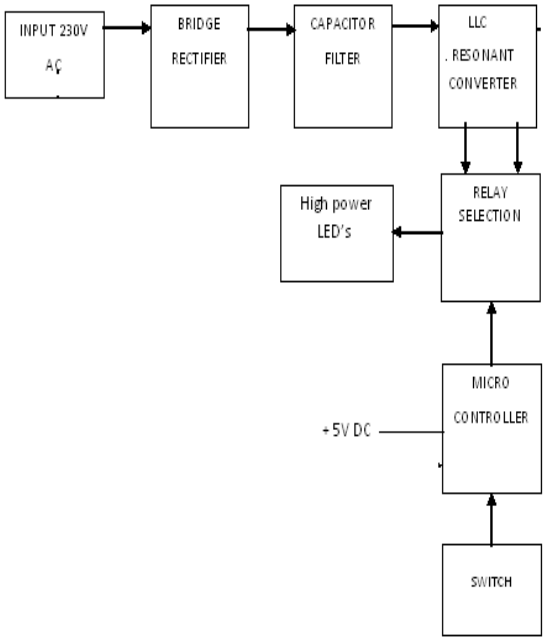

Figure 2: Block diagram of Proposed LED driver

In most of the circuits the relay is often driven by transistor or MOSFET. To make a relay operate, you have to feed suitable pull-in and holding current (DC) through its energizing coil. And generally relay coils are designed to operate from a particular supply voltage. Commonly used relays are often 12V or 5V, in the case of many of the small relays used for electronics work. Relay's supply voltage ranges from 5V to 24V. In each case the coil has a resistance which will draw the right pull-in and holding currents when it is connected to that supply voltage. So the basic idea is to choose a relay with a coil designed to operate from the supply voltage for control circuit and then provide a suitable relay driver circuit so that low-power circuitry can control the current through the relay's coil. Typically this will be somewhere between 25mA and 70mA.

A relay coil is not only an electromagnet but it's also an inductor. When power is applied to the coil the current in the coil builds up and levels off at its rated current, depends on the DC resistance of the coil. Some energy is now stored in the coil's magnetic field. When the current in the coil is turned off this stored energy has to go somewhere. The voltage across the coil quickly increases trying to keep the current in the coil flowing in the same direction. This voltage spike can reach hundreds or thousands of volts and can damage electronic parts. by adding a flyback diode the current has a path to continue flowing through coil until the stored energy is used up. The diode also clamps the voltage across the coil to about 0.7V protecting the electronics. The stored energy dissipates quickly in the diode. The current stops flowing and the relay turns off. The diode should be able to handle the coil current for a short time and switch relatively fast.

Microcontroller AT89C51 is an 8-bit microcontroller and belongs to Atmel's 8051 family. ATMEL 89C51 has 4KB of Flash programmable and erasable read only memory and 128 bytes of RAM. It can be erased and program to a maximum of 1000 times. In 40 pin AT89C51, there are four ports designated as P_1, P_2, P_3 and P_0. All these ports are 8-bit bi-directional ports, *i.e.*, they can be used as both input and output ports. Except P_0 which needs external pull-ups, rest of the ports have internal pull-ups. When 1s are written to these port pins, they are pulled high by the internal pull-ups and can be used as inputs. These ports are also bit addressable and so their bits can also be accessed individually. Port P_0 and P_2 are also used to provide low byte and high byte addresses, respectively, when connected to an external memory. Port 3 has multiplexed pins for special functions like serial communication hardware interrupts, timer inputs and read/write operation from external memory. AT89C51 has an inbuilt UART for serial communication. It can be programmed to operate at different baud rates. Including two timers & hardware interrupts it has a total of six interrupts switch to select voltages.

III. HARDWARE IMPLEMENTATION OF THE PROPOSED LLC RESONANT CONVERTER FOR HIGH POWER LED DRIVER

The hardware implementation of the proposed LED driver mainly consists of LLC resonant converter, micro controller for selecting the output voltage level using relays for driving of the higher power LEDs. The power supply requirement for each unit is explained in further details. In the proposed LED driver microcontroller gets 5V Dc power supply from 230V mains supply. The mains voltage is stepped down and given to the rectifier circuit along with the filter section as shown in Fig 3. Hence a dc of 16V approximately is derived from this section. This is applied to the regulator section. +5V constant Dc supply is obtained from the regulator IC. Micro controller IC senses the input through two pins of the port1. Namely p1.0 and p1.1. The relay selection is done through the output port p2.0 and p2.1. The relays are activated through a transistor BC547. The relays used are single change over 12V relays. Two different voltages like 12V and 110V are switched as per the need of the load. The load LEDs are connected in series. Each LED consumes 2W of power. For an input voltage of 110V, when 44 LEDs are connected in series, it dissipates totally 88 watts of power approximately. When 12V output supply is selected, 8W of power is dissipated in LEDs shown in Fig 5&Fig 6. In order to avoid heating of LEDs, They have been mounted on an aluminium based heat sink. The controller codings have been written in assembly language ASEM software. While assembling the codings of our project, it generates, two files namely, led.hex and led.lst files. Our interest is to load the hexa codes into the chip, hence, led.hex is burnt into the 89c51 micro controller through the ATMEL flash programmer from pc to the chip via a serial port RS232C standard cable.

The main supply of 230V supply is rectified and filtered through smoothing capacitor to provide approximate 320V DC to the input terminals of LLC resonant converter as shown in Fig 3 & Fig 4, 1k potentiometer connected to the base of the transistor BC369 gets the base drive, which is nothing but the error between the reference voltage and the available voltage. This error voltage drives the transistor BC369 and whose collector voltage is used to drive the transistor c1815. The base voltage is developed at c1815 is based on the timing pulses created by the RC circuit, whose time period is given by 0.0015 micro farad and 5 k ohms of resistor. So total time period = $7.5x10^{-6.}$ So switching frequency will be f=133.33 kHz. After this pulses are applied to the MOSFET circuit, it gets drives and the primary of the transformer is driven and the secondary output is obtained. This voltage is now rectified through a diode and filtered through the capacitor. The DC is now available to drive the LEDs. The LEDs used in the proposed high power LED driver circuit consumes 2W each. Hence, the total power dissipated in the LEDs is near 80w. Through a micro controller, we will be able to select the amount of power dissipated in two levels. It can be like 80w or 8w.The load LEDs are connected in series as shown in Fig 4. Electrically connecting the LEDs in series circuit combinations reduces the power consumption. All the LEDs connected in series pass the same current so it is best if they are all the same type. The power supply must have sufficient voltage to provide about 2V for each LED plus at least another 2V for the resistor. In order to avoid heating of LEDs, They have been mounted on an aluminium based heat sink.

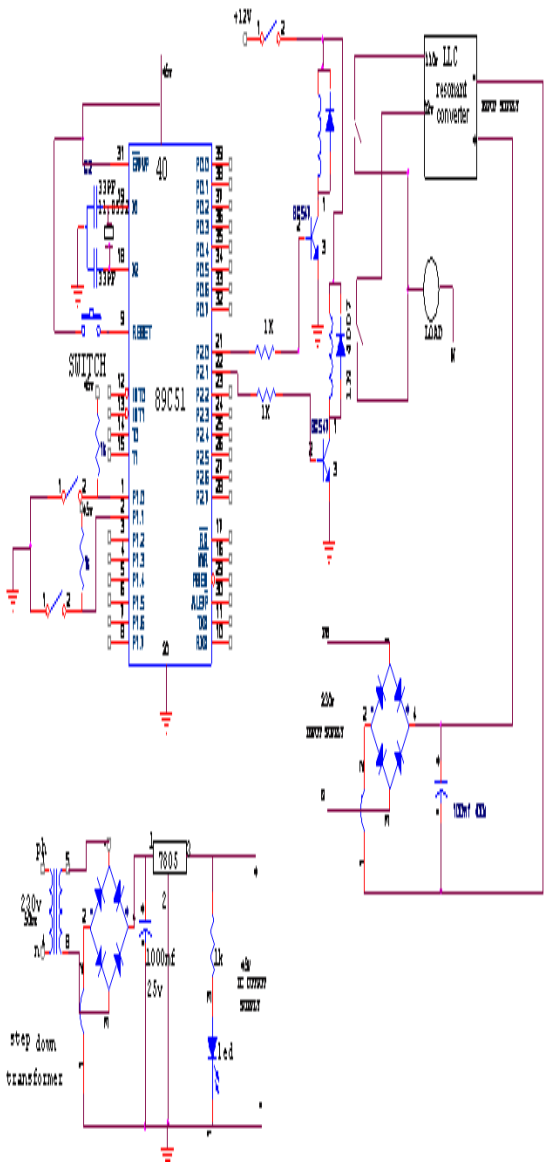

Figure 3. The proposed LED driver

LEDs are current-driven which means that the intensity of the light they generate depends on the amount of electric current flowing them. The voltage drop across an LED depends entirely on the current flowing through it and ranges from 2-4 Volts for most LEDs. Typically current is controlled using a resistor in series with the LED, or a current regulator circuit. Supplying more current to an LED increases its intensity, and reducing the current decreases its intensity. One way of dimming an LED is to use a variable resistor (potentiometer). In the proposed driver dimming is mainly achieved through variable resistor (potentiometer) for to dynamically adjust the current getting to the LED and therefore increasing or decreasing its intensity

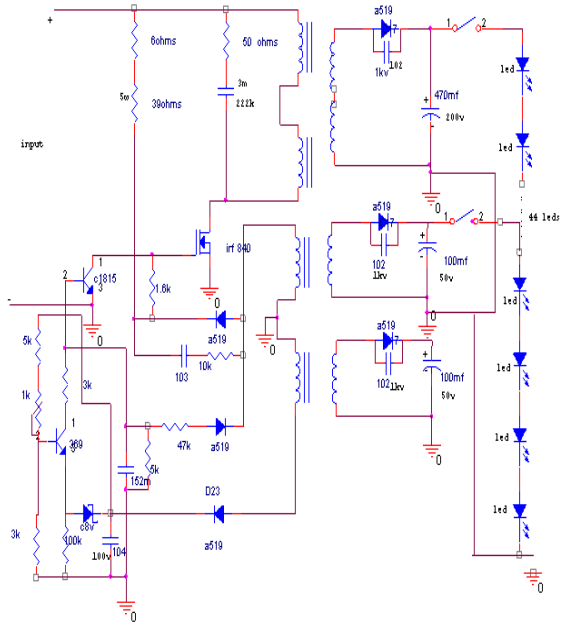

Figure 4. LLC resonant converter for driving high power LEDs

V. EXPERIMENT RESULTS

In this paper, a prototype 88W high power LED driver is built and tested for supplying 44 LEDs (in five parallel paths and eight LEDs in series connection for each parallel path and in sixth parallel path includes 4 LEDs). In addition, each LED's rated power is 2 W, and its forward voltage Vf is about 3.2~3.4 V. Fig. 5 Photo of lighting the LEDs, that are utilizing the proposed driver for lightening of the 8W of LEDs by selecting 12V output supply from LED driver and Fig 6 Photo of lighting the LEDs, that are utilizing the proposed driver for lightening of the 88W of LEDs by selecting 110V output supply from LED driver. Circuit specifications of the proposed driver as shown in Table 1. specification and parameters of switch and microcontroller as shown in Table 2.

Table 1: Circuit specifications

Input voltage V_{in}	230 VAC
Output voltage V_o	110 VDC
Output power P_o	88 W
Switching frequency	133.33 KHZ

Table 2: Specification and Parameters

Switch	MOSFET (IRF840) 500V,8A
Control IC	
Microcontroller	AT 89C51

Fig. 5 Photo of lighting the LEDs, that are utilizing the proposed driver for lightening of the 8W of LEDs by selecting 12V output supply from LED driver

Fig. 6 Photo of lighting the LEDs, that are utilizing the proposed driver for lightening of the 88W of LEDs by selecting 110V output supply from LED driver

VI. CONCLUSION

This paper has proposed a LLC resonant converter for high power LED driver for supplying high-power LEDs, which combines LLC resonant converter,relay selection with microcontroller provides an option for selecting of the output voltages is mainly drawn from LLC resonant converter to drive high power LEDs.The proposed driver also controls the brightness of the LED lightening through dimming technique. Here dimming is mainly achieved through by varying the potentiometer on the driver circuit. A 88W prototype high power LED driver has been developed and tested with 230V input utility-line voltage, which provides cost-effective LEDs driver with high power factor, low total harmonic distortion of input utility-line current and zero-voltage-switching on power switches, all of which result in high efficiency.

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PREDICTION OF PROTEIN STABILITY BY SUPPORT VECTOR MACHINES

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Abstract— The primary goal in protein engineering is development, production and storage of stable proteins with full functionality. Any protein can be characterized by stability determination and the force that leads to stability. The stability of protein depends on the interaction between amino acid side chains (dipeptide bonds). In this research work, we have developed a machine learning system to classify stable and unstable proteins using support vector machines (SVMs). 50,000 protein sequences were collected from the Protein Data Bank (PDB) and the stability associated data were obtained from the Expasy tools. A set of SVMs was trained to predict the stability of a given protein based on its amino acid and the amino acid pairs. On 5-fold cross-validation, the SVM gave a maximum classification accuracy of 98%. An improvement in the prediction accuracy was identified over the algorithm which was based on the amino acid composition alone.

Keywords—*Machine Learning, SVMs, Instability Index, ProtParam, PDB*

I. INTRODUCTION

Proteins are organic macromolecules, recognized by smaller units called amino acids. They are essential parts of all living organisms as they participate in every process within cells [1, 2]. Aminoacids are classified based on their side chain properties. The side chain makes the amino acid, weak acid or weak base and hydrophilic or hydrophobic [3]. These monomers are joined together by the peptide bonds that constitute the primary structure of protein molecules and a pair of aminoacids results in a dipeptide. The sequence continues with the formation of tripeptides, tetrapeptides, pentapeptides, and so on [4, 5].

Each of the side chain of amino acid can link to 19 other amino acids to create a total of 39 different dipeptide bonds. Permuting this for other residues resulted in a total of 780 combinations of dipeptides. If other peptide bonds are also considered, the number of combinations reaches to a very large number. However, on studying the protein sequences from database, it is found that all the amino acid residues do not occur with equal frequency in all the proteins and the natural sequence does not reflect even a small percentage of all mathematical possible combinations [6].

The structure of proteins can be obtained by representing amino acids in a flat two dimension of polypeptide chains. However, it is important to represent proteins in three-dimensional arrangement to stress the spatial arrangement of amino acid residues or more precisely, as the overall topology formed by the polypeptides. A protein fold arises by linking together the secondary structures forming a compact globular molecule [7]. The formation of stable tertiary fold depends on the attractive interaction of dipeptide bonds in the protein. Protein stability is thermodynamically described by the standard Gibbs energy change, ΔG, concerned with unfolding the distinctive, three dimensional structure to randomly coiled polypeptide chains. Though, for building the new proteins or improving stability of existing proteins, understanding of the overall ΔG is not adequate [8]. Relatively it is enviable to have factors in hand that allows estimation of the various contributions to stability of individual interactions resulting from amino acid substitutions. This research work, helps in identifying the stable proteins from the given protein sequences [9]. The capability of living organisms are marked by extreme conditions like pH (1-12), temperature (-5 - 110°C), hydrostatic pressure (0.1 - 120 MPa) and water activity (0.6 - 1.0) as shown in Fig.1. While organisms existing at extreme

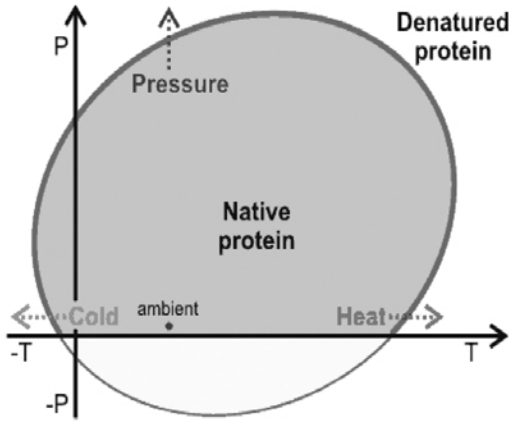

Figure 1. Variation of the stability of the proteins with external conditions

pH usually maintain neutral pH in their cytoplasm by active proton pumps, other extremophiles, such as

thermophilic or barophilic organisms, cannot escape the external stress but have to adapt for survival. Important candidates for adaptational changes are proteins that carry out many of the important tasks in living cells [10]. As a result there is great interest in understanding the stabilization of the native structure of proteins due to their great importance in rational protein design in medical and technical applications.

Protein structures are stabilized by non-covalent intramolecular interactions between amino acid side chains. Protein complexes are formed by specific non-covalent intermolecular interactions. Most of the biological processes depend on proteins being stable and in the appropriate folded conformation [11]. It is important to identify the stability of the protein molecules as it gives insight to the protein folding problem in their biologically active states, and how these active states are stabilized. Many factors are responsible for the folding and stability of native proteins, including hydrophobic interactions, hydrogen bonding, conformational entropy, and the physical environment. There have been quick advances in structural biology and relating structure or sequence to biochemical function and mechanism [12].

The complete characterization of any protein requires stability identification and the forces which direct to stability and correct folding.

Various physical, statistical and machine learning approaches are generally used to predict the stability of proteins. ProtParam [13] is an online tool that predicts the stability of proteins using statistical analysis of dipeptide bond combinations in the given protein sequence. It gives the stability of a protein sequence by computing instability index value for the given protein sequence [14]. The instability index is calculated based on the 400 dipeptide combinations, each of which is assigned an instability weight value.

In this research work, a machine learning system to predict the stability of proteins using SVMs has been developed. A set of 50,000 protein structures were taken from Protein Data Bank (PDB) [15]. PDB is a database containing information about experimentally identified structures of proteins, nucleic acids and complex assemblies. It also contains various tools and resources that help the users to perform simple and advanced searches queries based on sequence, structure and function. The PDB repository contains around 60,000 protein sequences with their structures. Of these 60,000 protein sequences, 50,000 were obtained from PDB in fasta format.

II. THEORITICAL BACKGROUND

Support vector machine (SVM) is a supervised learning machine, which classifies each input data set into one of the two classes of data namely positively labelled and negatively

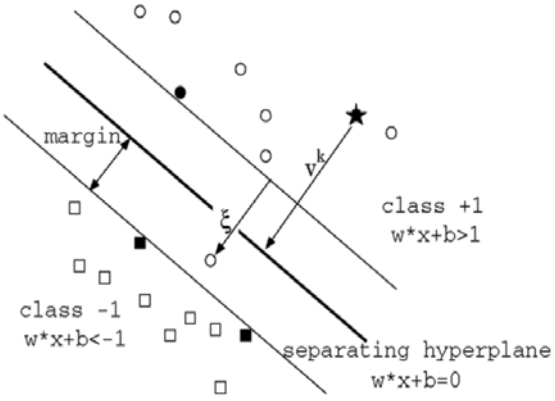

Figure 2. Mapping of input vectors by SVM

labelled classes. SVMs are the algorithms that belong to the category of supervised learning methods [16]. The SVM learning algorithm builds a model which classifies the new example into one of the two labeled classes. An SVM model is a representation of each point in vector spaces with a hyperplane that separates the points in positively labelled classes with those in the negatively labeled classes [17]. SVMs construct a hyperplane or a set of hyperplanes in a multi dimensional space. An SVM is capable of representing nonlinear relationships and producing models that generalize well to unseen data (Fig.2).

SVMs can be trained with a parameter called complexity parameter(C), also known as capacity parameter, for the purpose of regulating overfitting. Choosing a decision boundary, that is extremely partial towards the training set and does not generalize well is called overfitting. For efficient classification, it is mandatory to choose the optimum complexity parameter. It determines the trade-off between choosing large-margin classifier and the amount by which wrongly classified samples are tolerated. A larger C value means that more priority is given to minimize the amount of misclassification than to finding a wide margin model [18]. There are many other parameters associated with the kernel, apart from the C value.

III. COMPUTATIONAL METHODOLOGY

In Protein Data Bank (PDB) altogether there were 62773 protein structures. Out of which 50,000 proteins were collected. Sequences with a high degree of similarity to other sequences were removed by all-to-all sequence similarity search using the program ALIGNs, which produces an optimal global alignment between two protein sequences. As a result 15,000 protein sequences which are having more than

90% similarity were removed using that technique. Fasta sequences for these proteins were acquired from PDB. Stability related data for all the proteins were retrieved from PDB and the Expasy tools [15]. Expasy Proteomic server enables for finding the stability of the protein from its aminoacid sequences. A major limitation for this Expasy tool is that it will find the properties of the protein sequences which are having moderate sequence length. Of the 35,000 validated data from PDB, 16524 proteins were found to be unstable and the rest 18,476 were stable.

As the classification is binary, SVM light has been used for learning and classification of data. SVM light is an implementation of SVMs in C language. The advantage of SVM light over other SVMs are it uses a fast optimization algorithm, solves classification and regression problems, allows restarts from specified vector of dual variables, computes error-rate, precision accuracy and accuracy on recall, handles thousands of support vectors, handles several hundred thousands of training examples, supports standard kernel function and allows the users to define their own.

As each protein sequence is made of amino acids, the feature values of each data set were selected as the number of amino acids and the number of dipeptides present in the protein sequence. There are 20 different amino acids and 400 possible dipeptides in a protein sequence. The feature values for each data set were extracted from each sequence. As a result altogether 420 features were extracted from the sequences.

The prepared dataset was subjected to SVM learning and classification and the prediction accuracy were identified. The prediction performance was inspected by the 5-fold cross validation test, in which the data set of 35000 was divided into five subsets of roughly equal size. This means that the entire data was divided into training and test data in five different ways. After training the SVM with a collection of four subsets, the performance of the SVM was tested using the fifth subset. This process is repeated five times so that each subset is once used as the test data.

The machine is trained by varying the C value – trade-off between training error and margin value on different data sets and prediction accuracy of the results are compared. The comparisons of all results obtained are carried out using a confusion matrix. A confusion matrix is a visualization tool used in supervised learning. A pictorial representation of confusion matrix is shown in Table 1,

TABLE I CONFUSION MATRIX

		Predicted	
		Negative	*Positive*
Actual	*Negative*	a	b
	Positive	c	d

where

- *a* is the number of correct predictions that an instance is negative;
- *b* is the number of incorrect predictions that an instance is positive;
- *c* is the number of incorrect predictions that an instance if negative;
- *d* is the number of correct predictions that an instance is positive

Various parameters of the efficiency like accuracy, recall, precision, etc. can be calculated using the confusion matrix. Accuracy is the proportion of the total number of predictions that were correct as in (1). Recall is the proportion of positive cases that were correctly identified as in (2) and precision is the proportion of the predicted positive cases that were correct as in (3).

$$ACCURACY = \frac{(a+d)}{(a+b+c+d)} \quad (1)$$

$$RECALL = \frac{d}{(c+d)} \quad (2)$$

$$PRECISION = \frac{d}{(b+d)} \quad (3)$$

IV. RESULTS AND DISCUSSIONS

Protein sequence data were collected from the PDB and the features were extracted. The total number of data taken for the analysis was 35000. The stability associated data were retrieved from PDB and Expasy tools. The entire dataset had two classes; Unstable and Stable proteins with 16524 and 18476 data respectively. The total number of features taken into account was 420.

The dataset was subjected to SVM and the prediction accuracy was found to be 83%. The prediction performance for the data set was validated by 5-fold cross validation test.

The accuracy of each test set data for various values of C values are shown in Table II. Each cell in the table shows the value of accuracy for a particular value of C in a particular data set. From the table, it is clear that the maximum value of prediction accuracy

is obtained from DataSet 4 for c=3 with a maximum prediction accuracy of 98%.

TABLE II PREDICTION ACCURACY FOR EACH DATASET AFTER 5-FOLD CROSS VALIDATION

C-Value	Prediction Accuracy On Test Datasets				
	DataSet1	*DataSet2*	*DataSet3*	*DataSet4*	*DataSet5*
0.01	92.30%	93.75%	93.60%	93.20%	93.95%
0.05	95.15%	96.60%	95.50%	94.95%	95.25%
0.1	94.95%	96.70%	95.65%	95.65%	95.75%
1	95.50%	97.00%	96.50%	96.80%	95.75%
2	95.55%	96.65%	96.80%	96.80%	97.00%
3	95.40%	96.35%	96.60%	**98.05%**	96.75%
4	95.55%	96.10%	96.70%	96.80%	96.75%
5	95.60%	96.10%	96.65%	97.00%	96.65%
6	95.50%	96.70%	96.85%	96.25%	96.15%
7	95.30%	96.10%	96.70%	96.70%	96.05%
8	95.40%	95.85%	96.70%	96.35%	96.05%
9	95.50%	96.45%	96.30%	95.90%	95.95%
10	95.60%	95.80%	96.35%	96.30%	95.60%
11	95.70%	95.65%	96.20%	96.15%	95.60%
12	95.70%	95.70%	96.00%	96.25%	95.70%
13	95.60%	95.85%	95.90%	95.20%	95.55%
14	95.50%	95.95%	95.95%	95.25%	95.80%
15	95.55%	95.05%	95.90%	95.15%	95.70%

By changing the complexity value C, better result for prediction accuracy can be obtained by increasing the margin classifier. But very large value for C prioritizes the amount of misclassification rather than finding a wide margin. Thus more data gets misclassified and the prediction accuracy reduces. Hence an optimal value for C must be chosen to get maximum prediction accuracy.

V. CONCLUSIONS

Machine learning technique helps in making prediction of protein stability effectively. SVM, which is considered as a common bioinformatics prediction tool gives 98% prediction accuracy for the data set. By this approach, a machine learning system has been developed to predict the stability of the proteins. The prediction tool requires only a minimum space while compared to huge databases. Altogether more than 35,000 data were taken into consideration. After performing cross validation and setting complexity parameter to an optimal value, results showed very good prediction accuracy. Results obtained manually using statistical methods matched with the machine learning approach. This method can be used as a reliable tool to classify stable and unstable proteins from their primary sequence alone.

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PRESENT SCENARIO ANALYSIS OF GREEN COMPUTING APPROACH IN THE WORLD OF INFORMATION TECHNOLOGY

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Abstract—Making the computing experience more and more "environmental friendly" is the new concern of the IT valleys of the world including India. Green computing refers to the "environmentally sustainable" computing or Information Technology. Green Computing talks in for the operation of computers and related peripherals in order to minimize the carbon footprint. This paper proposes its focus towards the practical implementations on changes that can result in more energy efficient consumption by the systems. Also, is discusses various factors that can enable green computing to be integrated into various aspects of our day to day lifestyle, classroom and research laboratories. Analysis has been done that juxtapose how *"going green"* is a benefit for the environment as well as a person or a business firm in-terms of cost saving and as well as performance. Solutions are discussed in terms of technological and economic evidence validating the benefits of "Going Green" and to promote education of *"Green Computing"* in the classroom, department and research lab or just at home to solace the cause in saving our planet earth. General terms: environment, energy, financial savings, planet earth.

Keywords: *Green computing; going green; environmentally sustainable; energy efficient.*

I. INTRODUCTION

The term ***"green"*** has always been associated with the name of something that is inclined towards the ***"nature"*** or something that has to do with the beneficiary of the environment. *"Going Green"* implies reducing your energy use and pollution footprint. **"Green computing"** in this context is growing as a popular term coined by the technology community of this world nowadays, which is aims at the effort of achieve the highest possible environmental sustainability by campaigning and implementing the best possible operation of the computers and its related peripherals to help minimize their adverse effects

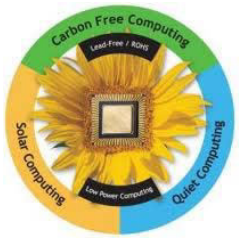

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Fig.1. Green Computing saves the environment.

While the goal of a truly paperless office has yet to be realized, it certainly began a movement towards Green Computing [1].

Green Computing primarily focuses but is not limited to the following aspects: ***These are virtualization, power management, power supply, storage, video card and e-materials recycling***. Evolution of virtualization is directly related to the practical implementations of green computing process. "*VMware*" is no strange name to using virtualization technologies for implementing energy and cost savings. With Information technology spanning our reliance on it, it has become in our best interest to think of its effective use while considering the environment as a priority concern. This paper is also a step forward in the same direction to offer insights into paths of Green Computing that incorporates computer science and information technology pupils to implement the techniques and following the practices and methods discussed in here would help achieving a much ***"greener computing environment"***. The various paradigms of Green computing have been analysed practically in here as well as the current efforts along with an empirical evaluation. This paper tries to solve the intricate associated with the approaches of a greener computing environment and its futuristic dimensions.

II. WHY GREEN COMPUTING AND WHY GO GREEN

A. Need

Newton's Third Law of Motion states that "For every action, there is an equal and opposite reaction.", similarly the consumption of energy sources has a negative reaction on the environment. The various departments of the IT sectors are continuously using a large amount of power and consequently regular cooling energy is needed to counteract this power usage. It can be an endless circle of energy waste. Hence, the three main reasons that made us realize the need for growing green are

1. Release of harmful gases from electronics.
2. More utilization of power and money.
3. Increase of E-waste and improper standalone pc's disposals.

Fig.2. Landfills due improper disposal of computers.

The present scenario of computing technology is solemnly focusing on providing customers with high performance with a low cost availability in market

However, this approach needs serious amendments because the longevity of environmental sustainability has to be maintained. This brings us to a need of green computing and making the computers friendly for the environment.

B. Motivation and approaches

The biggest problem arising out of the new generation PC's is that most of them are run underutilised and then after some time are changed with a new one. Today's PC's are so powerful that they use only a small amount of their capacity. A single PC generates more heat than a 100 watt bulb. Schools, colleges and offices using PC generally keep them in an air conditioned room [6]. According to IDC research quoted by VMware on their green computing site, the lack of server consolidation using virtualization costs American businesses more than $140 Billion dollars, with more than 20 million servers producing more than 80 million tons of CO2 per year [2]. Those figures claim to represent more CO2 emissions than the country of Thailand and more than half of all the countries in South America [2].

Computer technology use accounts for 2% of anthropogenic CO2, roughly equivalent to aviation industry. The IT energy usages will double next 4 years [3]. For every 12 consumers who keep power settings enabled for their on their monitors and PCs, CO2 emissions equivalent to removing one average automobile from the road will be avoided [3].

A typical desktop ***PC with a 17-inch LCD monitor requires about 145 watts—110 watts for the computer and 35 watts for the monitor***. If left on 24x7 for one year, this same computer will consume 1,270 kilowatt hours of electricity—that's enough to release 1,715 pounds of carbon dioxide into the atmosphere and the equivalent of driving 1,886 miles in the average car! [3].

III. PARADIGMS OF A GREENER COMPUTING- AN ANALYSIS

The major paradigms of green computing approach, followed in a broader way are:

A. Power management and energy efficiency

The biggest issue related to power management is the energy efficient Data center designs. Data center facilities are heavy consumers of energy, accounting for between 1.1% and 1.5% of the world's total energy use in 2010 [7].

[CHART 1]

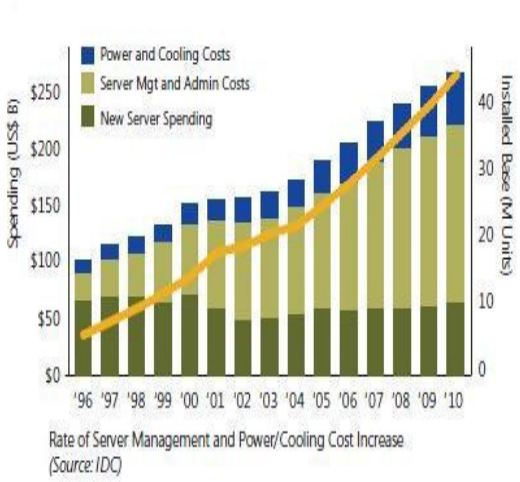


Chart.1 .Data center costs

This explains how the cost of maintaining the data centers with has increased in the past years. Report says that by 2020 the emissions from data-centers and services over the Internet are expected to grow even larger than that of aviation in terms of their carbon footprints [8]. Energy efficient data center design use virtualization and similar technique to better utilize a data center's space, and increase performance and efficiency while reducing the power as well as costs.

B. Choice of eco-friendly hardware and efficient software.

According to the Climate Group, total energy consumption by computers – including the power consumption and embodied energy of data centers, PCs and peripherals, and networks and devices – accounted for 830 million metric tons of carbon dioxide, or 2 percent of the total world carbon footprint, in 2007. As Figure 1 shows, these figures are roughly equivalent to the total CO2 emissions of Nigeria, Iran, and Poland, respectively. Data centers alone use almost 0.5 percent of the world's energy, and this figure is likely to quadruple by 2020.

[CHART 2]

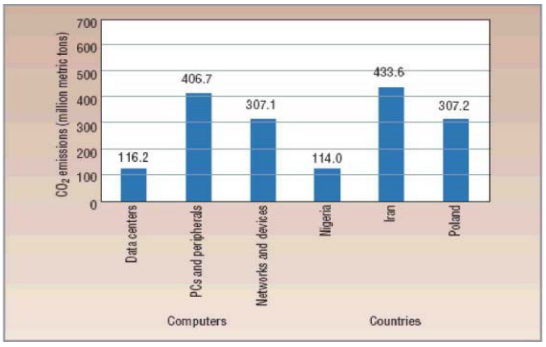


Chart. 2. Carbon dioxide emissions from the energy consumed by data centers, PCs and peripherals, and networks and devices are roughly equivalent to those of Nigeria, Iran, and Poland and account for 2 percent of the total world carbon footprint.

Lowering the energy cost of computation as well as their carbon footprints depends on various hardware and software features such as reducing the processor cycles, communication needs, and architectural inefficiencies. In this regard, The Energy Star program has a standard, nowadays found in all electronic devices . It rates various devices according to their energy efficiency.

Fig. 3.The Energy Star Logo

Hardware advances provide new opportunities for compile-time or dynamic efficiency improvement. For example, heterogeneous chip multiprocessors can achieve four to six times energy savings per instruction [9]. Recent advancements have also been done that show even higher energy savings, even up to 100 times.

C. Material recycling and increasing the product life

Electronic items that are considered to be hazardous include, but are not limited to:

1. Televisions and computer monitors that contain cathode ray tubes

2. LCD desktop monitors
3. Laptop computers with LCD displays
4. LCD televisions
5. Plasma televisions and portable DVD players with LCD screens.

The E-waste in India is expected to rise 500% by 2020. Not only will India see a 500% increase in e-waste, but other countries like China and South Africa will see a 400% increase from 2007 levels over the next ten years, with mobile phones being a significant component, rising 7 times higher in China and 18 times higher in India[4]. Large amounts of e-waste are sent to countries such as China, India and Kenya, where lower environmental standards and working conditions make processing e-waste more profitable. Around 80% of the e-waste in the U.S. is exported to Asia [5]. Not only the above mentioned items but other related peripherals such as hard disks, printers and other internal parts can be recycled in a judicious manner and can be reused again in an effort to avoid the land fillings and improper disposals that are otherwise going to be greatest upcoming trouble on the planet earth.

D. Others

Opting for an eco-friendly computing also greatly influences factors like cost effectiveness and saving energy as well as money.

TABLE.1
INDIAN STATE ELECTRICITY TARIFFS
(DOMESTIC)

State	Tariff effective from	Domestic (Rs./kWh)
Madhya Pradesh	06-08-2009	5.62
Mumbai (Reliance En.)	01-06-2009	5.58
Gujarat	01-02-2009	5.55
Andhra Pradesh	01-04-2009	3.97
Delhi	07-06-2009	3.52
BYPL/BRPL/NDPL Delhi NDMC	01-07-2009	2.54
Chhattisgarh	01-07-2009	2.31

TABLE.1. shows the some electricity tariffs in different states of India in decreasing order. In an office, a lab, a classroom or just at home computers and its related peripherals are left on *standby* all the time. Many electrical devices exhibit phantom load of 1-3 watts due to lack of any physical switch. This may look a small figure but a constant draw of this much power by AC/DC adapters or a LAN-friendly wake up functionality available of computers causes a large amount of power consumption that goes into waste.

The following equation will approximate the cost that in a system that has 15 electrical devices, each each drawing a *standby power* of as little as 3 watts when "off," will incur in one year:

$$Power_{year} = \frac{15\ devices * 3\ Watts * 24\ hours * 365\ days}{1000}\ kWh \quad (1)$$

This results in an annual consumption of *394.3 kWh* of *standby power* that is consumed as waste. Taking the electricity rates from Table 1 if this system would be in *Madhya Pradesh* then at the rate of Rs. *5.62/kWh*, the total cost of phantom load for this system is about *Rs. 2215.4/year.* Of course the rates have gone much higher in since then.

IV. PLAUSIBLE APPROACHES AND APPLICABLE PRACTICES

A. Busting of the myths

There have been many myths associated with the computers and their usage.

The four very common costly computer myths found are:

1. You should never turn off your computer: Your computer is designed to handle 40,000 on/off cycles. If you are an average user, that's significantly more cycles than you will initiate in the computer's five-to seven- year-life. When you turn your computer off, you not only reduce energy use, you also lower heat stress and wear on the system.

2. Better to leave your computer ON than to turn it off and "power ON" back again: There is nothing common between an automobile and a personal computer that it would suck enormous energy every time it is turned on. The surge of power used by a CPU to boot up is far less than the energy your computer uses when left on for more than three minutes.

3. Screen savers save energy: One of the most common misconceptions regarding the screen savers is that they can save energy when the computer is in idle but in reality, it is not. The fact is that screen savers were originally designed to help prolong the life of monochrome monitors and these monitors are now technologically obsolete. Screen savers save energy only if they actually turn off the screen or, with laptops, turn off the backlight but mostly they don't do so.

4. You may lose your network connections if your computer goes into low-power/sleep mode: Computers today are designed to sleep on networks without loss of data or connection. CPUs with Wake on LAN (WOL) technology can be left in sleep mode overnight to wake up and receive data packets sent to the unit.

B. Reconsidering the use of single processing systems

While the computer system developments are resulting in more and more advance and faster processing systems, the frequency chart of the number of computers being underutilized are increasing exponentially. Single processing units can be used in places where there are number of small tasks needed to be processed at different times or simultaneously. A single processing system therefore can be reconsidered for use as the newer computers today have very high speed processors that in performance terms are otherwise left underutilised only. For a general PC consisting of at least a CPU machine and a CRT monitor an LCD screen , the single processing system enables the completion of the same tasks at a given or a bit more time but consuming a very small amount of energy as compared to that used by 10 or 20 different standalone PC's.

C. Upgrading efficient hardware and recycling old ones

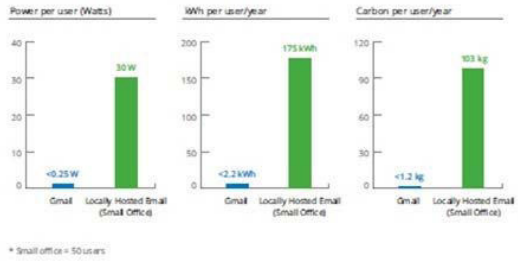
As mentioned above the E-waste in India is expected to rise 500% by 2020. Not only in India but also the rest of the world is on a verge of suffering with the great tragedy of landfills of e-wastes. Today, a personal computer or any electronic device retire very early and the need of a better option can be required in a very short term notice as a new breakthrough in technology happens every day in the IT sector. In this situation, an efficient hardware up gradation as per the need would be a much generous choice for a user than to replace the old system with a brand new one. Doing this will not only increase an individual computer's lifecycle but is also a major step forward toward green computing. Also, peripherals such as hard disks, printers and other internal parts can be recycled in a judicious manner and can be reused again in an effort to avoid the land fillings and improper disposals that are otherwise going to be greatest upcoming trouble on our planet.

D. Eliminating the vampire load

As shown by the empirical evaluation above, the phantom loads or the vampire loads suck up a shocking amount of energy. Eliminating the phantom load can be highly cost-effective as well as eco-friendly too. The solution to the phantom load problem is to pull the plug from the wall when the electrical device is not in use [10], with a more convenient alternative being the use of a switchable power strip. More sophisticated power strip devices sometimes called as the *smart strips* are available that can automatically power off any devices plugged into the strip when a specific device, such as the computer, is powered off [11].

V. FUTURISTIC INSIGHTS OF AN ECO-FRIENDLY COMPUTER WORLD

Google has shown for years that the cloud can deliver a high-quality, reliable, and useful service at a much lower energy cost than other methods. File storage, calendar, teleconferencing, voicemail, chat and document management all enjoy these energy economies.



Graph 1.Locally hosted server vs Gmail. Comparison of power, energy and carbon use (Google survey).

Even traditional applications such as word processing and spreadsheets may ultimately benefit if users transition from traditional PCs and laptops to lower energy devices like tablets or netbooks that score their information in the cloud [12]. Cloud based services are growing. Email, movies, music, television and telephone services increasingly rely on cloud computing to serve, store and transmit data [12]. As these technologies develop and mature, efficient hardware, software, and server provisioning will continue to make the cloud the most energy efficient platform for delivering computing even more efficient is the future of green computing.

VI. CONCLUSION AND FUTHER DISCUSSION

Incorporating the Green Computing approaches strategies analysed in this paper can have an immediate impact on the grass root level that beholds the Green Computing approach. This analysis of Green Computing under the current scenario of the Information technology in the world showed that green computing strategies are not that hard to implement as critics' claim it to be. Also going green can be cost effective too on many supporting grounds. Various methods and plausible approaches analysed in this paper shows how efficiently Green Computing can be implemented in order to sustain in harmony with the environment while advancing our technical capabilities simultaneously. Common practices discussed here including the "myths" and the phantom load tells us how following some simple steps in the cliché can prove vital to our green computing attempts in the long run. Also, the futuristic insights of green computing envision the efforts that are already started by IT giants such as Google, Microsoft. This paper directly implies the inevitability of a greener computing environment in the future and the right technologies that are need to be advanced in order to achieve a proper blend of IT approach in harmony with the nature.]

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COMPARISON OF DENOISING FILTERS ON COLOUR TEM IMAGE FOR DIFFERENT NOISE

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Abstract— TEM (Transmission Electron Microscopy) is an important morphological characterization tool for Nano-materials. Quite often a microscopy image gets corrupted by noise, which may arise in the process of acquiring the image, or during its transmission, or even during reproduction of the image. Removal of noise from an image is one of the most important tasks in image processing. Denoising techniques aim at reducing the statistical perturbations and recovering as well as possible the true underlying signal. Depending on the nature of the noise, such as additive or multiplicative type of noise, there are several approaches towards removing noise from an image. Image De-noising improves the quality of images acquired by optical, electro-optical or electronic microscopy. This paper compares five filters on the measures of mean of image, signal to noise ratio, peak signal to noise ratio & mean square error. In this paper four types of noise (Gaussian noise, Salt & Pepper noise, Speckle noise and Poisson noise) is used and image de-noising performed for different noise by various filters (WFDWT, BF, HMDF, FDE, DVROFT). Further results have been compared for all noises. It is observed that for Gaussian Noise WFDWT & for other noises HMDF has shown the better performance results.

Keywords— *Nanomaterials, Noise, Denoising, Filters, Qualit.*

I. INTRODUCTION

Image denoising can be considered as a component of processing or as a process itself. Image denoising involves the manipulation of the image data to produce a visually high quality image. Images get often corrupted by additive and multiplicative noise. In today's real time applications and requirements resolution we get from normal images is not sufficient[1]. We need look insight its crystallographic structure, topography, morphology etc of a substance. As nanoscopic image has got wide and significant use in the medical research and applications and in many other domains. Due to acquisition TEM images contain electronic noise and white diffraction artifacts localized on the edges of the Nanomaterials Various types of filters have been proposed for removal of noise in these microscopic images. Filtering is the most popular method to reduce noise. In the spatial domain, filtering depends on location and its neighbours. In the frequency domain, filtering multiplies the whole image and the mask. Some filters operate in spatial domain, some filters are mathematically derived from frequency domain to spatial domain, other filters are designed for special noise, combination of two or more filters, or derivation from other filters [2, 8]. An early and very popular approach was to achieve filtering in the frequency domain, just by trimming high-frequency components of the image spectrum. The Wiener filter is the MSE-optimal stationary linear filter for images degraded by additive noise and blurring. Wiener filters are often applied in the frequency domain Wiener filters are unable to reconstruct frequency components which have been degraded by noise. This computationally fast method has however a major drawback: it tends to smooth out the salient features of the signal, such as edges and textures [4]. Wavelets and other transformations in a combined space-frequency domain nicely address this issue and lead to very efficient filtering schemes. In wavelet thresholding, a signal is decomposed into its approximation (low-frequency) and detail (high-frequency) sub-bands; since most of the image information is concentrated in a few large coefficients, the detail s sub-bands are processed with hard or soft thresholding operations[9,10,11]. This methodology constitutes an important achievement in the field of the edge preserving denoising algorithms, suitable to deal with the discontinuities associated with anatomical details. The median filter provides a mechanism for reducing image noise, while preserving edges more effectively than a linear smoothing filter [5]. Many common image-processing techniques such as rank-order and morphological processing are variations on the basic median algorithm, and the filter can be used as a steppingstone to more sophisticated effects. However, due to existing algorithms' fundamental slowness, its practical use has typically been restricted to small kernel sizes and/or low-resolution images [3, 13].Traditional filtering is domain filtering, and enforces closeness by weighing pixel values with coefficients that fall off with distance. Similarly, we define range filtering, which averages image values with weights that decay with dissimilarity. Range filters are nonlinear because their weights depend on image intensity or color. Bilateral Filter is the combination of both domain and range filters. Total variation denoising (TV) is a special case of image regularization methods that balances a smoothness measure and a fidelity term [6, 12]. This paper discusses the major types of noises, various types of filters applied on a nanoscopic image. It discusses the performance of each filter on a nanoscopic image by making comparisons on the

basis of certain image quality metrics like mean , mean square error, signal to noise ratio & peak signal to noise ratio.

II. NOISE IN AN MICROSCOPIC IMAGE

We define noise as an unwanted component of the image. Noise occurs in images for many reasons. Noise can generally be grouped into two classes, independent noise & the noise which is dependent on the image data. Additive noise is evenly distributed over the frequency domain (i.e. white noise), whereas an image contains mostly low frequency information. Hence, the noise is dominant for high frequencies and its effects can be reduced using some kind of lowpass filter. This can be done either with a frequency filter or with a spatial filter. (Often a spatial filter is preferable, as it is computationally less expensive than a frequency filter.)In the second case of data-dependent noise (e.g. arising when monochromatic radiation is scattered from a surface whose roughness is of the order of a wavelength, causing wave interference which results in image speckle), it is possible to model noise with a multiplicative, or non-linear, model. These models are mathematically more complicated; hence, if possible, the noise is assumed to be data independent.

A. Gaussian Noise

Gaussian noise is characterized by adding to each image pixel a value from a zero-mean Gaussian distribution. The zero mean property of the distribution allows such noise to be removed by locally averaging pixel values [1]. Noise is modelled as additive white Gaussian noise (AWGN), where all the image pixels deviate from their original values following the Gaussian curve. That is, for each image pixel with intensity value O_{ij} ($1 \le i \le M$, $1 \le j \le N$ for an M x N image), the corresponding pixel of the noisy image X_{ij} is given by,

$X_{ij}=O_{ij}+G_{ij}$ (1)

Where, each noise value G is drawn from a zero –mean Gaussian distribution. Gaussian noise can be reduced using a spatial filter. However, it must be kept in mind that when smoothing an image, we reduce not only the noise, but also the fine-scaled image details because they also correspond to blocked high frequencies.

B. Poisson Noise

Poisson noise, is a basic form of uncertainty associated with the measurement of light, inherent to the quantized nature of light and the independence of photon detections. Its expected magnitude is signal-dependent and constitutes the dominant source of image noise except in low-light conditions. The magnitude of poisson noise varies across the image, as it depends on the image intensity.

C. Salt & Pepper Noise

Another common form of noise is *data drop-out* noise (commonly referred to as *intensity spikes*, *speckle* or *salt and pepper noise*). Here, the noise is caused by errors in the data transmission. The corrupted pixels are either set to the maximum value (which looks like snow in the image) or have single bits flipped over. In some cases, single pixels are set alternatively to zero or to the maximum value, giving the image a `salt and pepper' like appearance. Unaffected pixels always remain unchanged. The noise is usually quantified by the percentage of pixels which are corrupted.[2]

D. Speckle noise

Increase in power of signal and noise introduced in the image is of same amount that is why speckle noise is termed as multiplicative noise [13]. It is signal dependent, non-Gaussian & spatially dependent. Due to microscopic variations in the surface, roughness within one pixel, the received signal is subjected to random variations in phase and amplitude. The variations in phase which are added constructively results in strong intensities while other which are added destructively results in low intensities. This variation is called as Speckle.[1]

III. DENOISING FILTERS

A. Bilateral Filter

Bilateral filtering is a non-linear filtering technique. It extends the concept of Gaussian smoothing by weighting the filter coefficients with their corresponding relative pixel intensities. Pixels that are very different in intensity from the central pixel are weighted less even though they may be in close proximity to the central pixel. This is effectively a convolution swith a non-linear Gaussian filter, with weights based on pixel intensities. This is applied as two Gaussian filters at a localized pixel neighbourhood, one in the spatial domain, named the domain filter, and one in the intensity domain, named the range filter. Bilateral filter compares the intensity of the pixel to be filtered with the surrounding filtered intensities instead of the noisy ones. [3]

Mathematically, at a pixel location x, the output of bilateral filter is calculated as shown in Fig.1

$$\tilde{I}(\mathbf{x}) = \frac{1}{C} \sum_{y \in N(x)} e^{\frac{-\|\mathbf{y}-\mathbf{x}\|^2}{2\sigma_d^2}} e^{\frac{-|I(\mathbf{y})-I(\mathbf{x})|^2}{2\sigma_r^2}} I(y)$$

Fig.1 Bilateral Filter Equation

where sigmad and sigma r are parameters controlling fall-off of weights in spatial and intensity domains respectively, N (x) is a spatial neighbourhood of pixel I (x), and C is the normalization constant. Bilateral Filter is not parameter free. The set of

bilateral filter parameters has an important influence on its performance and behaviour.

B. Weiner Filter using DWT

Wiener filter minimizes the mean square error between the uncorrupted signal and the estimated

$$W(f_1, f_2) = \frac{H^*(f_1, f_2) S_{xx}(f_1, f_2)}{|H(f_1, f_2)|^2 S_{xx}(f_1, f_2) + S_{\eta\eta}(f_1, f_2)},$$

where $S_{xx}(f_1, f_2)$, $S_{\eta\eta}(f_1, f_2)$ are respectively power spectra of the original image and the additive noise, and H(f1,f2) is the blurring filter. Discrete Wavelet Transform analyzes the signal by successive use of low pass and high pass filtering to decompose the signal into its coarse and detail information. By taking only a limited number of highest coefficients of the discrete wavelet transform, an inverse transform (with the same wavelet basis) more or less denoised signal can be obtained. [9]It is very effective because of its ability to capture energy of signal in few energy transform values.[10] This denoising algorithm de-noise image using Wiener filter for Low frequency domain and using soft thresholding for de-noise High-frequencies domains. This approach is gives better results than (DWT or Wiener) de-noising. [4]

C. Hybrid Median Filter

Median filter is widely used in digital image processing for removing noise in digital images. Although it does not shift edges, the median filter does remove fine lines and detail, and round corners. A more advanced version of this filter, which avoids these problems, is the hybrid median. Hybrid median filtering preserves edges better than a NxN square kernel-based median filter because data from different spatial directions are ranked separately [13]. Three median values are calculated in the NxN box: MR is the median of horizontal and vertical R pixels, and MD is the median of diagonal D pixels. The filtered value is the median of the two median values and the central pixel C: median ([MR, MD, C]). [5]

$$\begin{bmatrix} D & * & R & * & D \\ * & D & R & D & * \\ R & R & DCR & R & R \\ * & D & R & D & * \\ D & * & R & * & D \end{bmatrix}$$

Fig. 3 Formulation of Filtered Value

D. Dual Vectorial ROF Filter

Regularity is of central importance in computer vision. Total variation preserves edges and does not requires any prior information about the blurred image computed. One approach is to replace norm $l2$ in Tikhonov Regularization with the norm l^1, i.e., the 1-norm of the first spatial derivation of the solution. This is called the total variation (TV) regularization. signal. The inverse filtering is a restoration technique for deconvolution, i.e., when the image is blurred by a known lowpass filter, it is possible to recover the image by inverse filtering or generalized inverse filtering. The orthogonality principle implies that the Wiener filter in Fourier domain can be expressed as This method will help to obtain the discontinuities or steep gradients in the restored image. This procedure minimizes the vectorial total variation norm.[6] VTV minimization model is based on the dual formulation of the vectorial TV norm. Let us consider a vectorial (or M-dimensional or multichannel) function u, such as a color image or a vector field, defined on a bounded open domain $\Omega \subset R^N$ as

$x \rightarrow u(x) := (u_1(x), \ldots, u_M(x)), \; u : \rightarrow R^M,$

$$\inf_{u} \sup_{|p|\leq 1} \left\{ < u, \nabla \cdot p >_{L^2(\Omega;\mathbb{R}^M)} + \frac{1}{2\lambda} \|f - u\|^2_{L^2(\Omega;\mathbb{R}^M)} \right\}$$

Fig. 4 Formulation of Vectorial TV Norm

Which is convex in u and concave in p and the set {|p|<=1} is bounded and convex.[11,12]

E. Fuzzy Histogram Equalization

It proposes a novel modification of the brightness preserving dynamic histogram equalization technique to improve its brightness preserving and contrast enhancement abilities while reducing its computational complexity. This technique, called uses fuzzy statistics of digital images for their representation and processing. Representation and processing of images in the fuzzy domain enables the technique to handle the inexactness of gray level values in a better way, resulting in improved performance. Besides, the imprecision in gray levels is handled well by fuzzy statistics, fuzzy histogram, when computed with appropriate fuzzy membership function, does not have random fluctuations or missing intensity levels and is essentially smooth. This helps in obtaining its meaningful partitioning required for brightness preserving equalization.[7]

IV. METHODOLOGY USED

The complete simulation is carried in Matlab. The original microscopic image is taken. Noise is added to the original image. Four types of noises are added namely gaussian noise, speckle noise, salt & pepper noise & poisson noise respectively. This distorted image is then filtered using some algorithm and is compared with the statistics of original image to interpret that to what extent filter is able to denoise the image as shown in Fig.2

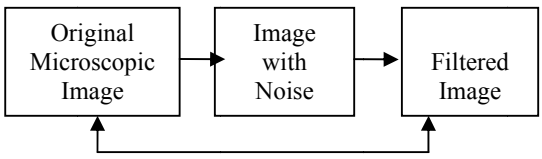

Fig. 5 Block Diagram

VI. SIMULATION RESULTS

A. Gaussian Noise

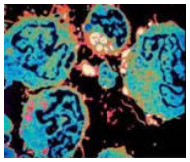

Fig.6 a Original

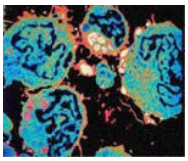

Fig 6b Noisy

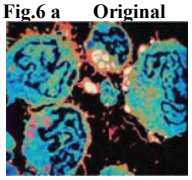

Fig 6 c WFDWT

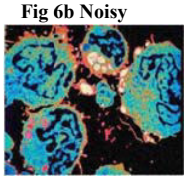

Fig 6d HMDF

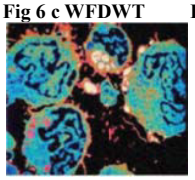

Fig 6e BF

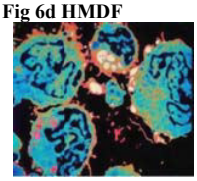

fig 6f DVROFT

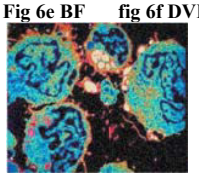

Fig 6g FDE

From fig. 6c when the image with gaussian noise is filtered using WFDWT , edges are preserved but are not sharp while when filtered using HMDFT & BF, images obtained are blurred in fig.6d & 6e , DVROFT filter preserves the edges sharply and removes the blurring effect from fig.6f.

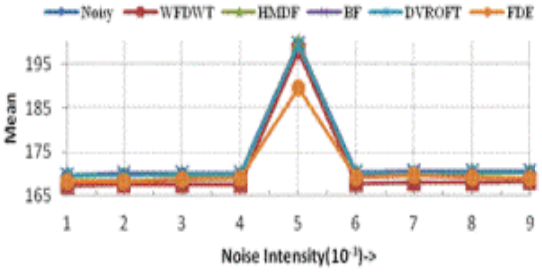

Fig. 7a Mean of Filtered Images with Gaussian Noise

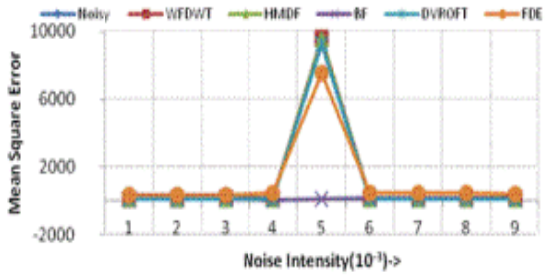

Fig. 7b MSE of Filtered Images with Gaussian Noise

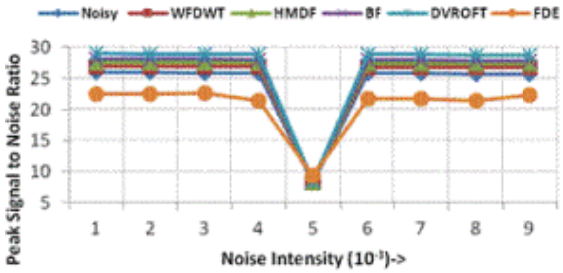

Fig. 7c PSNR of Filtered Images with Gaussian Noise

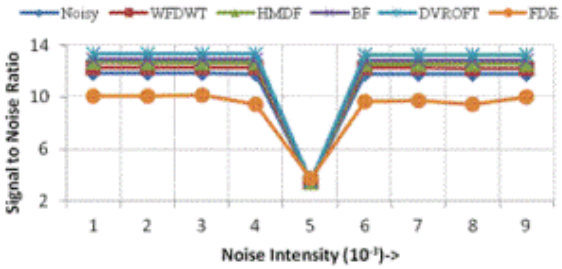

Fig. 7d SNR of Filtered Images with Gaussian Noise

When noise is introduced in the image the mean of image increased. When filtered with WFDWT, the mean is reduced significantly.The mean squared error (MSE) for our practical purposes allows us to compare the "true" pixel values of our original image to our degraded image. The MSE represents the average of the squares of the "errors" between our actual image and our noisy image. The error is the amount by which the values of the original image differ from the degraded image. Fig. 7b shows that BF gives the minimum value. Higher the SNR better is the reconstructed image, from Fig 7d, for nanoscopic image with gaussian noise , DVROFT filter gives the maximum value. Higher the PSNR, the better degraded image has been reconstructed to match the original image and the better the reconstructive algorithm. This would occur because we wish to minimize the MSE between images with respect the maximum signal value of the image. Fig. 7c depicts that BF gives the maximum value.

B. Speckle Noise

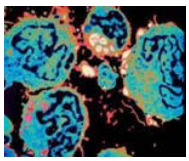

Fig 8a Original

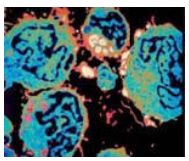

fig 8b Noisy

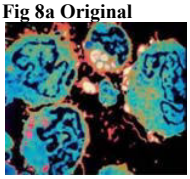

Fig 8cWFDWT

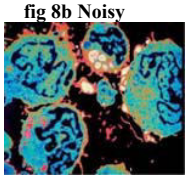

fig 8d HMDF

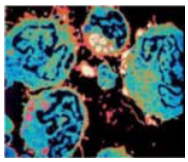

Fig 8e BF

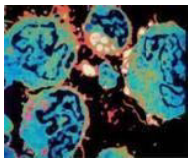

fig 8f DVROFT

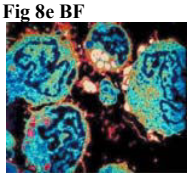

Fig 8g FDE

From fig. 8c to 8g it is clear that nanoscopic image with speckle noise is best filtered by HMDF.

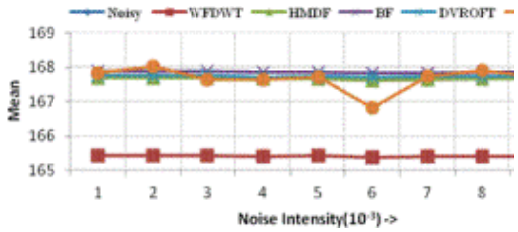

Fig. 9a MEAN of Filtered Images with Speckle Noise

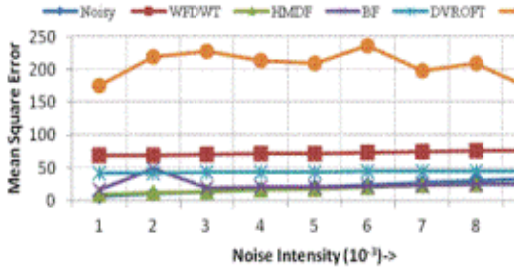

Fig. 9b MSE of Filtered Images with Speckle Noise

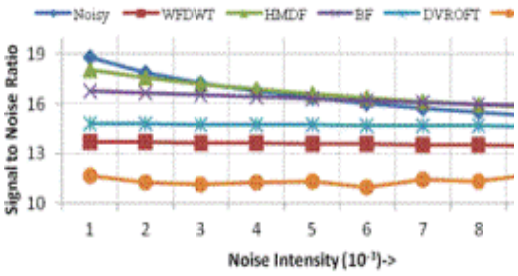

Fig. 9c SNR of Filtered Images with Gaussian Noise

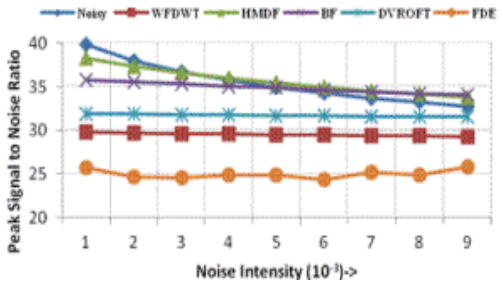

Fig. 9d PSNR of Filtered Images with Speckle Noise

Fig. 9a depicts that WFDWT gives the minimum value. Fig. 9b depicts that HMDF gives the minimum value. Fig. 9c depicts that HMDF gives the maximum value. Fig. 9d depicts that HMDF gives the maximum value.

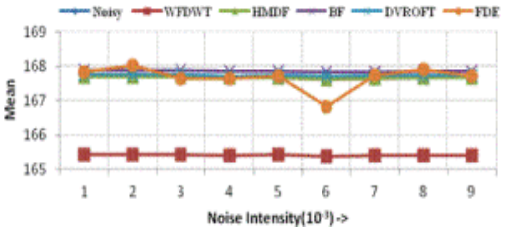

Fig. 9a MEAN of Filtered Images with Speckle Noise

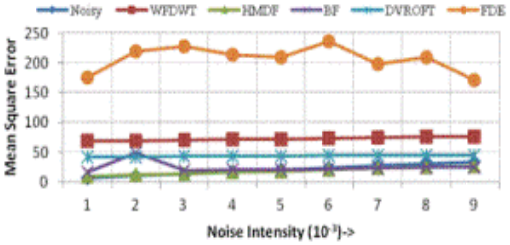

Fig. 9b MSE of Filtered Images with Speckle Noise

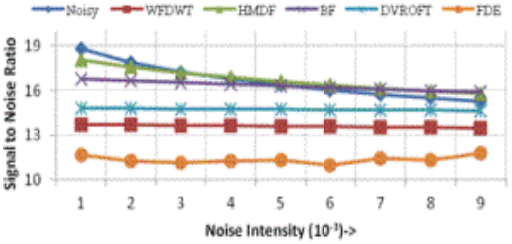

Fig. 9c SNR of Filtered Images with Gaussian Noise

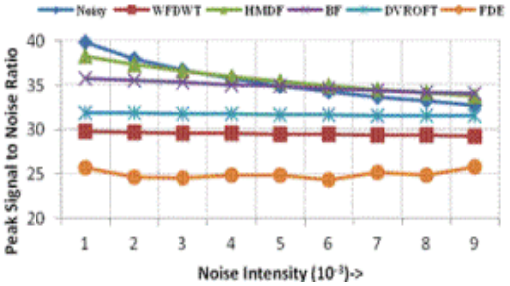

Fig. 9d PSNR of Filtered Images with Speckle Noise

Fig. 9a depicts that WFDWT gives the minimum value. Fig. 9b depicts that HMDF gives the minimum value. Fig. 9c depicts that HMDF gives the maximum value. Fig. 9d depicts that HMDF gives the maximum value.

C. Salt & Pepper Noise

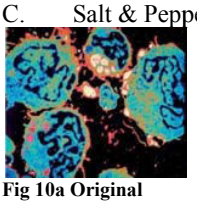

Fig 10a Original

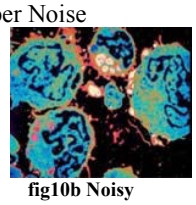

fig10b Noisy

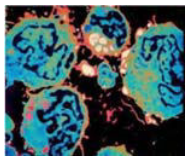
Fig 10c WFDWT

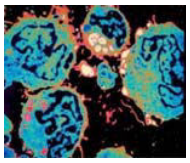
fig 10d HMDF

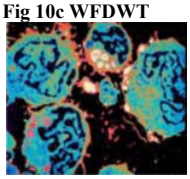
Fig 10e BF

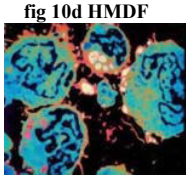
Fig 10f DVROFT

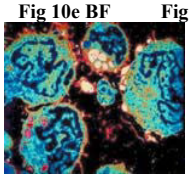
Fig 10g FDE

From fig. 10a to 10g it is clear that image with salt & pepper noise is best removed by HMDF.

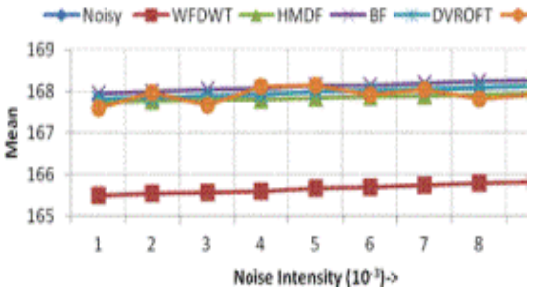

Fig. 11a MEAN of Filtered Images with Salt & Pepper Noise

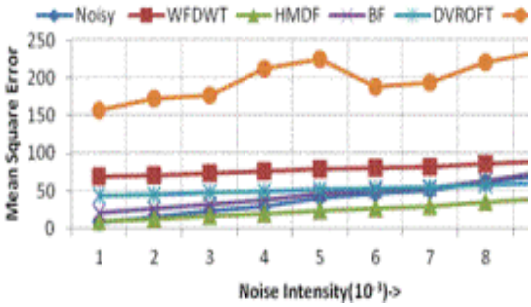

Fig. 11b MSE of Filtered Images with Salt & Pepper Noise

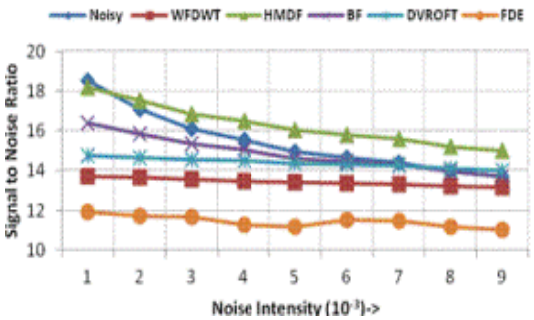

Fig 11c SNR of Filtered Images with Salt & Pepper Noise

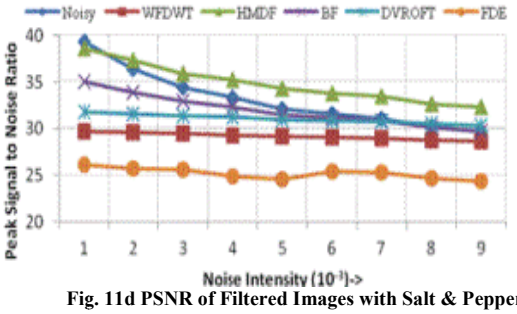

Fig. 11d PSNR of Filtered Images with Salt & Pepper Noise

Fig. 11a depicts that HMDF gives the minimum value. Fig. 11b depicts that HMDF gives the minimum value. Fig. 11c depicts that HMDF gives the maximum value. Fig. 11d depicts that HMDF gives the maximum value.

D. Poisson Noise

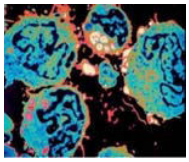
Fig 12a original

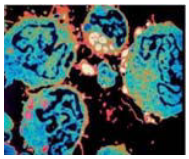
fig 12b noisy

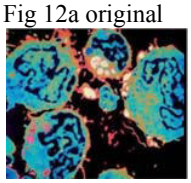
Fig 12c WFDWT

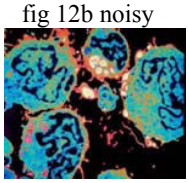
fig 12d HMDF

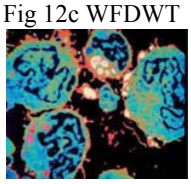
Fig 12e BF

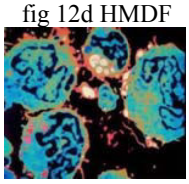
fig 12f DVROFT

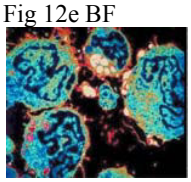
Fig 12g FDE

From fig. 12c to 12g it is clear that HMDF performs the best on nanoscopic image with poisson noise.

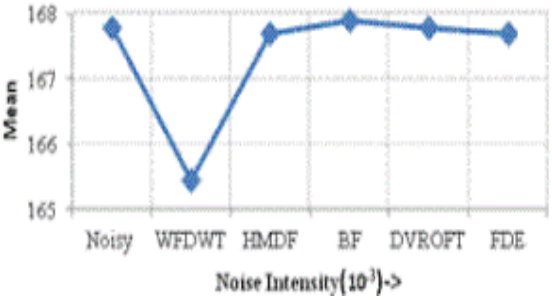

Fig. 13a Mean of Filtered Images with Poisson Noise

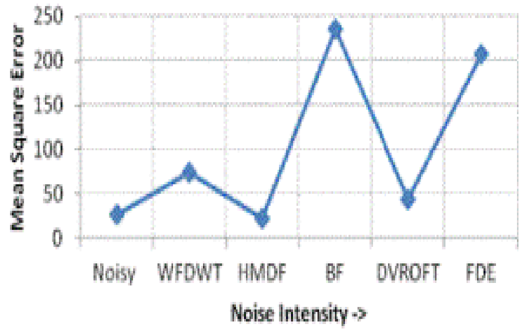

Fig. 13b MSE of Filtered Images with Poisson Noise

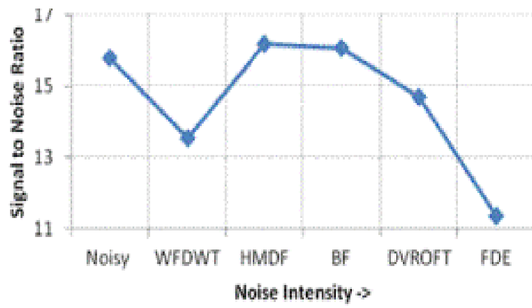

Fig 13c SNR of Filtered Images with Poisson Noise

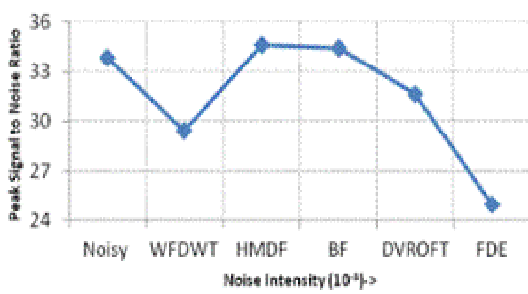

Fig. 13d PSNR of Filtered Images with Poisson Noise

From Fig.13, it is clear that WFDWT better reduces the mean value of the image while HMDF keeping the minimum MSE gives the maximum SNR & PSNR.

IV. CONCLUSION

An Image is denoised with four types of noise. For each type of noise the noise intensity variation taken is 0.001 to 0.009 i.e 1% to 9% . For each of these images four parameters Mean, MSE, SNR & PSNR are measured . Table 1 to Table 4 shows the averaged values. From Fig 6 to Fig 13, & Table 1 to Table 4 it is clear that for colour nanoscopic image with

a) Gaussian noise DVROFT filter has better performance.
b) Speckle , Salt & pepper and Poisson Noise HMDF has the better performance.

The conclusion is shown in Table 5

TABLE 5

	Gaussian Noise	Speckle Noise	Salt & Pepper Noise	Poisson Noise
MEAN	WFDWT	WFDWT	WFDWT	WFDWT
MSE	BF	**HMDF**	**HMDF**	**HMDF**
SNR	DVROFT	**HMDF**	**HMDF**	**HMDF**
PSNR	DVROFT	**HMDF**	**HMDF**	**HMDF**

V. FUTURE SCOPE

Though Dual Vectorial ROF Filters retains the structure in the image with high SNR & PSNR as compared when implemented on normal images but there is a blurring along edges as observed from Fig.3, 7 9 & 11. Hybrid Filter de-noise the image but affects the sharpness of edges. In all the results obtained images lost the actual color along the edge due to smoothing. Further these algorithms can be modified to overcome these drawbacks.

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TABLE 1

MEAN RESULTS	Gaussian Noise	Speckle Noise	Salt & Pepper Noise	Poisson Noise
Noisy	173.24	167.74	167.98	167.77
WFDWT	**171.06**	**165.41**	**165.65**	**165.44**
HMDF	173.19	167.67	167.84	167.70
BF	173.52	167.86	168.12	167.90
DVROFT	173.25	167.74	167.98	167.77
FDE	171.13	167.68	167.91	167.68

TABLE 2

MEAN SQUARE ERROR RESULTS	Gaussian Noise	Speckle Noise	Salt & Pepper Noise	Poisson Noise
Noisy	1207.38	20.68	38.19	26.70
WFDWT	1184.00	72.39	78.49	74.22
HMDF	1161.46	**18.42**	**23.45**	**22.36**
BF	**102.51**	24.73	44.97	235.62
DVROFT	1103.38	43.70	51.20	44.40
FDE	1204.36	206.62	197.95	206.85

TABLE 3

SIGNAL TO NOISE RATIO RESULTS	Gaussian Noise	Speckle Noise	Salt & Pepper Noise	Poisson Noise
Noisy	10.89	16.61	15.44	15.81
WFDWT	11.29	13.59	13.42	13.53
HMDF	11.60	**16.72**	**16.30**	**16.19**
BF	11.84	16.32	14.85	16.07
DVROFT	**12.22**	14.72	14.39	14.69
FDE	9.15	11.35	11.45	11.34

TABLE 4

PEAK SIGNAL TO NOISE RATIO RESULTS	Gaussian Noise	Speckle Noise	Salt & Pepper Noise	Poisson Noise
Noisy	23.92	35.47	33.14	33.87
WFDWT	24.80	29.54	29.20	29.43
HMDF	25.34	**35.70**	**34.85**	**34.64**
BF	**25.83**	34.90	31.96	34.41
DVROFT	26.62	31.73	31.06	31.66
FDE	20.63	25.00	25.20	24.97

◈◈◈

DISTRIBUTED ROUTING CONFIGURATIONS FOR IP NETWORK RECOVERY

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Abstract:- Now a day, Internet plays a major role in our day to day activities e.g., for online transactions, online shopping, and other network related applications. Internet suffers from slow convergence of routing protocols after a network failure which becomes a growing problem. Multiple Routing Configurations [MRC] recovers network from single node/link failures, but does not support network from multiple node/link failures. In this paper, we propose Enhanced MRC [EMRC], to support multiple node/link failures during data transmission in IP networks without frequent global re-convergence. By recovering these failures, data transmission in network will become fast.

Keywords: Re-convergence, Routing Instability, Proactive Mechanism, Failure Recovery.

I. INTRODUCTION

A network failure is happen in our network while communication, the traditional intra-domain routing protocols like OSPF is responds for the network-re convergence. In the Fast Reroute mechanism the failure is happen in the network, the all router present in the network are independently calculate the new routing tables for the response to the Failure happens in the network [3]. It is a time consuming process., because a failure happen in the network all the routers that are responds to the failure in the network and all routers are calculate the new routing tables for the response to the failure happen in the network. For this Fast Reroute mechanism we use the concept of multi-topology (MT) and use the network management concept based on introducing multiple logical topologies. For this multi topology routing is well suited for implementation of fast network recovery in our network In this mechanism uses the back up topologies for recover the network based on Fast Reroute. The enhanced IP Fast Reroute scheme which we call "relaxed MRC". It is increases the routing flexibility in each topology [2]. In this each link must be isolated in a back up topologies. The best mechanism for the network recovery in our communication infrastructure is the "Multiple Routing Configurations" for Fast IP network recovery in our communications. The powerful mechanism i.e., MRC is developed based on the concept of the Fast Reroute and the concept of relaxed MRC. The MRC isused to recover all single failure scenarios in our communication.

II. MRC FLOW

MRC is based on building a small set of backup routing configurations, that are used to route recovered traffic on alternate paths after a failure. The backup from the normal routing configuration in that link weights are set so as to avoid outing traffic in certain parts of the network. We observe that if all links attached to a node are given sufficiently high link weights, traffic will never be routed through that node. The failure of that node will then only affect traffic that is sourced at or destined for the node itself. Similarly, to exclude a link (or a group of links) from taking part in the routing, we give it infinite weight. The link can then fail without any consequences for the traffic. Our MRC approach is threefold. First, we create a set of backup configurations, so that every network component is excluded from packet forwarding in one configuration. Second, for each configuration, a standard routing algorithm like OSPF is used to calculate configuration specific shortest paths and create forwarding tables in each router, based on the configurations. The use of a standard routing algorithm guarantees loop-free forwarding within one configuration. Finally, we design a forwarding process that takes advantage of the backup configurations to provide fast recovery from a component failure.In our approach, we construct the backup configurations so that for all links and nodes in the network, there is a configuration where that link or node is not sed to forward traffic. Thus, for any single link or node failure, there will exist a configuration that will route the traffic to its destination on a path that avoids the failed element. Also, the backup configurations must be constructed so that all nodes are reachable in all configurations, i.e., there is a valid path with a finite cost between each node pair. Shared Risk Groups can also be protected, by regarding such a group as a single component that must be avoided in a particular configuration. In Sec. III, we formally describe MRC and how to generate configurations that protect every link and node in a network. Using a standard shortest path calculation, each

router creates a set of configuration-specific forwarding tables. For simplicity, we say that a packet is forwarded according configuration, meaning that it is forwarded using the forwarding table calculated based on that configuration. It is important to stress that MRC does not affect the failure- free original routing, i.e., when there is no failure, all packets are forwarded according to the original configuration, where all link weights are normal. Upon detection of a failure, only traffic reaching the failure will switch configuration. All other traffic is forwarded according to the original configuration as normal. If a failure lasts for more than a specified time interval, a normal re-convergence will be triggered. MRC doesnot interfere with this convergence process, or make it longer than normal. However, MRC gives continuous packet forwarding during the convergence, and hence makes it easier to use mechanisms that prevents micro-loops during convergence, at the cost of longer convergence times [12]. If a failure is deemed permanent, new configurations must be generated based on the altered topology .

III. GENERATING BACKUP CONFIGURATIONS

In this section, we will first detail the requirements that must be put on the backup configurations used in MRC. Then, we propose an algorithm that can be used to automatically create such configurations. The algorithm will typically be run once at the initial start-up of the network, and each time a node or link is permanently added or removed. **A. Configurations Structure**

MRC configurations are defined by the network topology, which is the same in all configurations, and the associated link weights, which differ among configurations. We formally represent the network topology as a graph G = (N, A), with a set of nodes N and a set of unidirectional links (arcs) A^1.

In order to guarantee single-fault tolerance, the topology graph G must be bi-connected. A configuration is defined by this topology graph and the associated link weight function.

Definition:

A configuration C_i is an ordered pair (G, w_i) of the graph G and a function

$$w_i : A \rightarrow \{1, \ldots, w_{max}, w_r, \infty\}$$

that assigns an integer weight $w_i(a)$ to each link a Є A.

We distinguish between the normal configuration C_0 and the backup configurations C_i, i > 0. In the normal configuration, C_0, all links have "normal" weights $w_0(a)$ Є{1, . . . , w_{max}}. We assume that C_0 is given with finite integer weights. MRC is agnostic to the setting of these weights. In the backup configurations, selected links and nodes must not carry any transit traffic. Still, traffic must be able to depart from and reach all operative nodes. These traffic regulations are imposed by assigning high weights to some links in the backup configurations:

Definition. A link a Є A is isolated in C_i if $w_i(a) = \infty$.

Definition. A link a Є A is restricted in C_i if $w_i(a) = w_r$.

Isolated links do not carry any traffic. estricted links are used to isolate nodes from traffic forwarding. The restricted link weight w_r must be set to a sufficiently high, finite value to achieve that. Nodes are isolated by assigning at least the restricted link weight to all their attached links. For a node to be reachable, we cannot isolate all links attached to the node in the same configuration. More than one node may be isolated in a configuration. The set of isolated nodes in C_i is denoted S_i, and the set of normal (non-isolated) nodes $S_i^1 = N \setminus S_i$.

Definition. A node u Є N is isolated in C_i if $\forall(u, v) \in A, w_i(u, v) \geq w_r$

$$\Lambda \quad \exists(u, v) \in A, w_i(u, v) = w_r \qquad (1)$$

With MRC, restricted and isolated links are always attached to isolated nodes as given by the following rules. For all links (u, v) Є A,

$$w_i(u, v) = w_r \text{ -> } (u \in S_i \Lambda v \in S_i^1) \text{ V } (v \in S_i \Lambda u \in S_i^1) \qquad (2)$$

$$w_i(u, v) = \infty \text{ -> } u \in S_i \text{ V } v \in S_i \quad (3)$$

The purpose of the restricted links is to isolate a node from routing in a specific backup configuration C_i, such as node 5 in FIGURE 1.a. In many topologies, more than a single node can be isolated simultaneously. In the example in IGURE 1.b. three nodes and three links are isolated. Restricted and isolated links are always given the same weight in both directions. EMRC guarantees single-fault tolerance by isolating each link and node in exactly one backup configuration. In each configuration, all node pairs must be connected by a finite cost path that

does not pass through an isolated node or an isolated link. A configuration that satisfies this requirement is called valid.

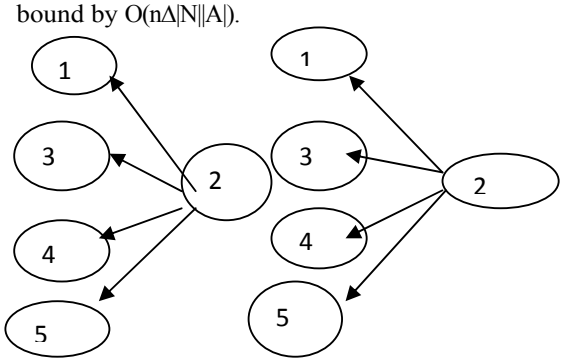
Termination:

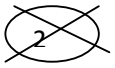
The algorithm runs through all nodes trying to make them isolated in one of the backup configurations and will always terminate with or without success. If a node cannot be isolated in any of the configurations, the algorithm terminates without success. However, the algorithm is designed so that any bi-connected topology will result in a successful termination, if the number of configurations allowed is sufficiently high.

Complexity:

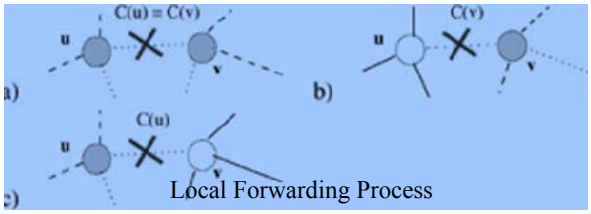
The complexity of the proposed algorithm is determined by the loops and the complexity of the connected method. This method performs a procedure similar to determining whether a node is an articulation point in a graph, bound to worst case O(|N|+|A|). Additionally, for each node, we run through all adjacent links, whose number has an upper bound in the maximum node degree Δ.

In the worst case, we must run through all n configurations to find a configuration where a node can be isolated. The worst case unning time for the complete algorithm is then bound by O(nΔ|N||A|).





Isolated nodes and links



Local Forwarding Process

When there is an error in the last hop u to a packet must be forwarded in the configuration where the connecting link is isolated. TThe figure shows isolated nodes (shaded color), restricted links (dashed), and isolated links (dotted). In cases (a) nd (b), c(u,v)= c(v) and the forwarding will be done in c(v). In case (c), c(u,v) not equal c(v), and the forwarding will be done in c(u)

IV. IMPLEMENTATION

The implementation of MRC for network recovery mainly uses three modules

1. Client Module 2. Sever Module 3. Router Module

1.Client :This module is used to send the data to server through routers. It will provide user friendly interface to send the data to the required destination.

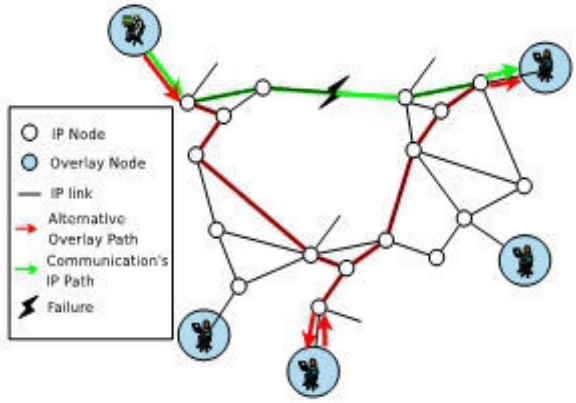
2. Server :It will receive the data send by the client which came from the active router. It can have any no. of clients.

3.Routers :These are placed in between server and client to transfer the data.

Whenever client send the data to the server it will pass through any one router. If the router is failed the data will be transferred through another router to reduce the system failure

Level 1 routing DFD

Context Level DFD



V.CONCLUSIONS

Multiple Routing Configurations [MRC] recovers network from single node and link failures,but does not support for multiple ode/link failures. Enhanced Multiple Routing Configurations [EMRC]is an approach to achieve fast recovery from multiple failures in IP Networks by using the timeslot mechanism. EMRC is based on providing the routers with additional routing information, allowing them to forward packets along routes that avoid a failed component. EMRC guarantees recovery from any failures in source to destination transmission, by calculating the alternate backup configurations in advance. After the occurrence of original route failure, it is not discarded before completion of timeslot.

Within the timeslot, if the failure is recovered, data is transmitted by using the original route. If the failure is not recovered; data is transmitted by using the backup route. During this transmission at any time, if the original route is recovered, data transmission using backup route is stopped and again shifted to the original route. By using this configuration one can improve the fastness of failure recovery and data transmission. EMRC thus achieves fast recovery with a very limited performance penalty.

EMRC does not take any measures towards a good load distribution in the network in the period when traffic is routed on the recovery paths. Existing work on load distribution in connectionless IGP networks has either focused on the failure free case or on finding link weights that work well both in the normal case and when the routing protocol has converged after a single link failure. Hence, EMRC leaves more room for optimization with respect to load balancing.

In spite of these encouraging results, this configuration is not to explain some of the issues those are like that this configuration can't develop for some multiple data failures at a time like occurrence of isolated nodes. It is recovered by improving the efficiency of isolated nodes by using the isolated links as restricted links.

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NEW VLSI ARCHITECTURE (HIGH THROUGH-PUT) SHORT BIT-WIDTH TWO'S COMPLEMENT MULTIPLIER

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Abstract—Two's complement multipliers are important for a wide range of applications (especially for signed, if the is in negative that nothing but two's complement no). In this paper we present a technique to reduce by one row the maximum height of the partial product array generated by a radix-4 Modified Boot Encoded multiplier, without any increase in the delay of the partial product generation stage. The proposed method can be extended to higher radices encodings, as well as any size *m £ n* multiplications. This reduction may allow a faster compression of the partial product array and regular layouts. This technique is of particular interest in all multiplier designs, but especially in short bit-width two's complement multipliers for high-performance embedded cores. We evaluate the proposed idea by providing first a gate equivalent study, and then through synthesis results. The comparisons with some other possible solutions show that the proposed approach is highly efficient in terms of both area and delay.

Index Terms—*Multiplication, Modified Partial Product Array, Low power design(less delay).*

1.INTRODUCTION

IN DSP and DIP(Maya)processing applications, performance, in most cases, strongly depends on the effectiveness of the hardware used ,which perform operation on low power (because power require ment is the essential factor in dsp applications)and produce less delay, for computing multiplications, since multiplication is, besides addition, massively used in these environments. The high interest in this application field is witnessed by the large amount of algorithms and implementations of the multiplication operation, which have been proposed in the literature (for a representative set of references see [2]). More specifically, short bit-width (8-16 bits) two's complement multipliers with single-cycle throughput and latency have emerged to be very important building blocks for high-performance embedded processors and DSP execution cores [3][4].Due to this here, in this paper I'm modifying the architecture which was introduced in[1].

In this case the multiplier must be highly optimized to fit within the required cycle time and power budgets. Another relevant application for short bit-width multipliers is the design of SIMD units supporting different data formats [4][5]. In this case, short bit-width multipliers often play the role to be basic building blocks. Two's complement multipliers of moderate bit-width (less than 32 bits) are also being used massively in FPGAs. All of the above translates into a high interest and motivation by the industry, to design highly performing short or moderate bit-width two's complement multipliers. The basic algorithm for multiplication is based on the well known paper and pencil approach [2] and passes through three main phases: *i)* partial product (PP) generation, *ii)* PP reduction and *iii)* final (carry propagated) addition. During PP generation a set of rows is generated, where each one is the result of the product of one bit of the multiplier by the multiplicand. For example, if we consider the multiplication $X £ Y$ with both X and Y on n bits and of the form $xn_i 1 : : : x0$ and $yn_i 1 : : : y0$, then the i_ith row is, in general, a proper left shifting of $y_i\ xX$, i.e. either a string of all zeros when $yi = 0$, or the multiplicand X itself when $y_i = 1$. In this case, the number of PP rows generated during the first phase is clearly n. Modified Booth Encoding (MBE) [5], [6], [7] is a technique which has been introduced to reduce the number of PP rows, still keeping both simple and fast enough the generation row one of the following possible values: all zeros, $+/-X;\ +/-2X$ [2].

The PP reduction is the process of adding all PP rows by using a compression tree [7], [8]. Since the knowledge of intermediate addition of values is not important, the outcome process of each row. One of the most commonly used schemes is radix-4 MBE, for a number of reasons, being the most important that it allows to reduce the size of the partial product array by almost half [5], and it is very simple to generate the multiples of the multiplicand. More specifically, the classical two's complement *nXn* bit multiplier using the radix-4 MBE scheme, generates a PP array with maximum height of $[n/2]+1$ rows, being each

TABLE 1: Modified Booth Encoding (Radix-4)

y_{2i+1}	y_{2i}	y_{2i-1}	Generated partial products
0	0	0	$0 \times X$
0	0	1	$1 \times X$
0	1	0	$1 \times X$
0	1	1	$2 \times X$
1	0	0	$(-2) \times X$
1	0	1	$(-1) \times X$
1	1	0	$(-1) \times X$
1	1	1	$0 \times X$

of this phase is a result represented in redundant carry save form, i.e., as two rows, which allows for much faster implementations. The last (carry-propagated) addition is the issue of adding these two rows and of producing the final result in a non redundant form, i.e., as a single row.

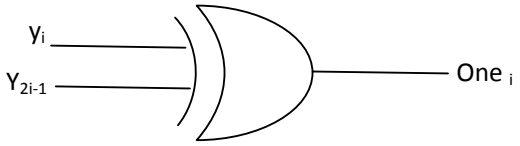
In this process, we introduce an idea to overlap, to some extent, the PP generation and the PP reduction phases. My aim is to generate a PP array with a maximum height of $\frac{n}{2}$ rows that is then going to reduce by the compressor tree stage. As we will see for the common case of values n which are power of two, the above reduction can reflect the implementation where the delay of the compressor tree is reduced by one XOR2 gate keeping a regular layout. Since we are focusing on small values of n and fast single-cycle units, this reduction must be important in cases where, for example, a high computation performance through the assembly of a huge number of small processing units with limited no of computation capabilities are required, such as 8×8 or 16×16 multipliers [9].

A similar study aimed at the reduction of the maximum height to $\frac{n}{2}$ but with different means has recently presented a interesting results in [10] and previously, by the same authors, in [11]. Thus, in the following, we will evaluate and compare the proposed approach with the technique in [2]. More details of our approach, besides the main results presented here, can be found in [12].

The paper is present s as follows: in Section 2, the multiplication algorithm based on MBE is briefly reviewed and analyzed. In Section 3, in this section the related work is presented here. In Section 4, present s the scheme to reduce the maximum height of the partial product array by one unit during the generation of the PP rows. Finally, in Section 5, presents evaluations and comparisons

.2.MODIFIEDBOOTH RECODED MULTIPLIERS

In general, a radix-$r = 2^k$ MBE leads to a reduction of the number of rows to about $\frac{n}{k}$ be while, on the other hand, it presents the need to



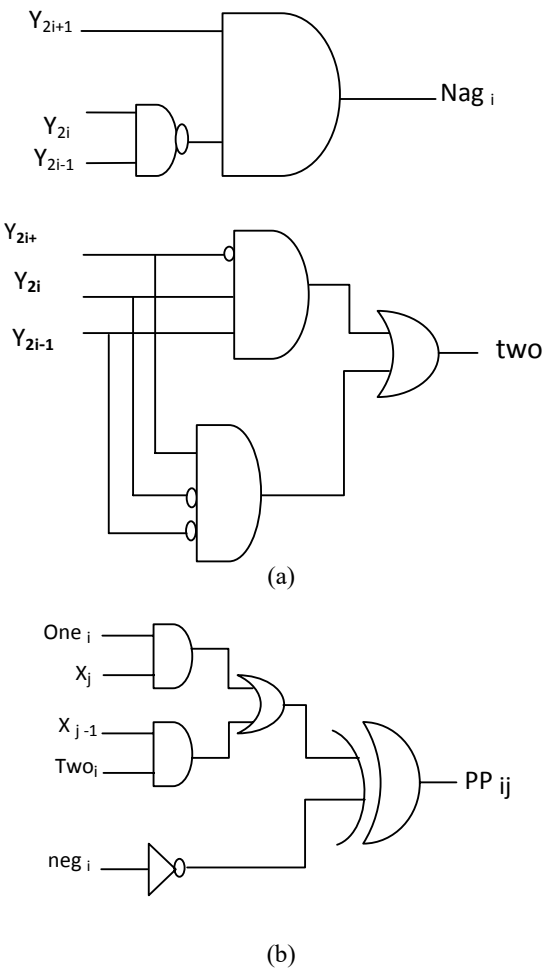


Fig. 1. Gate-level diagram for partial product generation using MBE (adapted from [2]). (a) MBE signals generation. (b) Partial product

generation.

generate all the multiples of the multiplicand X, at least from -B=$\frac{n}{2^k}$X to B/2 x X. As mentioned earlier , radix-4 MBE is particularly of interest since, for radix-4, it is easy to create the multiples of the multiplicand 0,$\pm X, \pm 2X$. In particular, $\pm 2X$ can be easily obtained by single left shifting of the corresponding terms$\pm X$ .It is clear that the MBE can be extended to higher radices (see [13] among others), but the advantage of getting a higher reduction in the number of rows is paid for by the need to generate more multiples of X. In this paper, we focus our attention on radix-4 MBE, although the proposed method can be easily extended to any radix-B MBE [13].

From an operational point of view, it is well known that the radix-4 MBE scheme consists of scanning the multiplier operand with a three-bit window and a

stride of two bits (radix-4). For each group of three bits (y2i+1, y2i, y2i_1), only one partial product row is generated according to the encoding in Table 1. A possible implementation of the radix-4 MBE and of the corresponding partial product generation is shown in Fig. 1, which comes from a small adaptation of [10, Fig. 12b]. For each partial product row, Fig. 1a produces the one, two, and neg signals. These signals are then exploited by the logic in Fig. 1b, along with the appropriate bits of the multiplicand, in order to generate the whole partial product array. Other alternatives for the implementation of the recoding and partial product generation can be found in [14], [15], [16], among others.

As introduced previously, the use of radix-4 MBE allows for the (theoretical) reduction of the PP rows to $\frac{n}{2}$, with the possibility for each row to host a multiple of $y_i \times X$ with $y_i \in \{\pm 0, \pm 1, \pm 2\}$. While it is straightforward to generate the positive terms 0, X, and 2X at least through a left shift of X, some attention is required to generate the terms -X and -2X which, as observed in Table 1, can arise from three configurations of the y2iþ1, y2i, and y2i_1 bits. To avoid computing negative encodings, i.e., -X and-2X, the two's complement of the multiplicand is generally used. From a mathematical point of view, the use of two's complement requires extension of the sign to the leftmost part of each partial product row, with the consequence of an extra area overhead. Thus, a number of strategies for preventing sign extension have been developed. For instance, the scheme in [1] relies on the observation that –pp= (~pp)= $pp - 1 - 2 + 4$. The array resulting from the application of the sign extension prevention technique in [1] to the partial product array of a 8×8MBE multiplier [7] is shown in Fig. 2.

The use of two's complement requires a neg signal (e.g., neg0, neg1, neg2, and neg3 in Fig. 2) to be added in the LSB position of each partial product row for generating the two's complement, as needed. Thus, although for a $n \times n$ multiplier, only $\frac{n}{2}$ partial products are generated, the maximum height of the partial product array is $\frac{n}{2}$. When 4-to-2 compressors are used, which is a widely used option due to the high regularity of the resultant circuit layout for n power of When 4-to-2 compressors are used, which is a widely used option due to the high regularity of the resultant circuit layout for n power of suitably connecting partial product rows and using a Wallace reduction tree [8], the additional delay can be further reduced to one XOR2 [17], [18]. However, the suppression

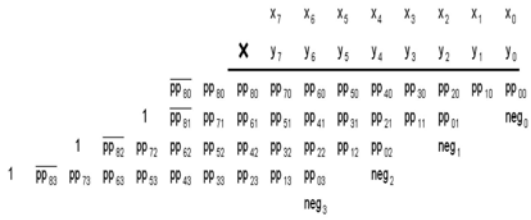


Fig. 2. Application of the sign extension prevention measure [2] on the partial product array of a 8 _ 8 radix-4 MBE multiplier.

still requires additional hardware, roughly a row of n half adders. This issue is of special interest when n is a power of two, which is by far a very common case, and the multiplier's critical path has to fit within the clock period of a high performance processor. For instance, in the design presented in [3], for n =16, the maximum column height of the partial product array is nine, with an equivalent delay for the reduction of six XOR2 gates [17], [18]. For a maximum height of the partial product array of 8, the delay of the reduction tree would be reduced by one XOR2 gate [17], [18].

Alternatively, with a maximum height of eight, it would be possible to use 4 to 2 adders, with a delay of the reduction tree of six XOR2 gates, but with a very regular layout.

3 RELATED WORK

Some approaches have been proposed aiming to add the $\left\lceil \frac{n}{2} \right\rceil + 1$ rows, possibly in the same time as the $\frac{n}{2}$ rows. The solution presented in [15] is based on the use of different types of counters, that is, it operates at the level of the PP reduction phase. Kang and Gaudiot propose a different approach in [10] that manages to achieve the goal of eliminating the extra row before the PP reduction phase. This approach is based on computing the two's complement of the last partial product, thus eliminating the need for the last neg signal, in a logarithmic time complexity. A special tree structure (basically an incrementer implemented as a prefix tree [18]) is used in order to produce the two's complement (Fig. 3), by decoding the MBE signals through a 3-5 decoder (Fig. 4a). Finally, a row of 4-1 multiplexers with implicit zero output1 is used (Fig. 4b) to produce the last partial product row directly in two's complement, without the need for the neg signal. The goal is to produce the two's complement in parallel with the computation of the partial products of the other rows with maximum overlap. In such a case, it is expected to have no or a small time penalization in the critical path. The architecture in [10],[19] is a logarithmic version of the linear method presented in [20] and [21]. With

respect to [20], [21], the approach in [10] is more general, and shows better adaptability to any word size. An example of the partial product array produced using the above method is depicted in Fig.5

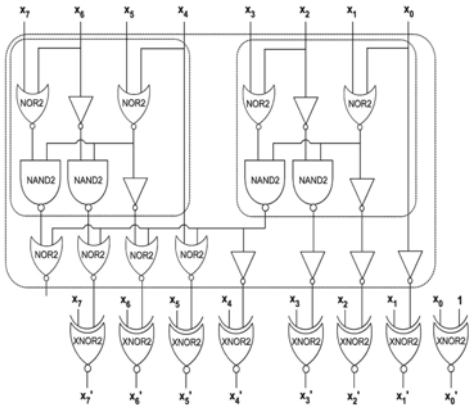


Fig. 3. Two's complement computation (n =8) [10].

This can be extend for more than 8 bit sequence .as is present in the circuit(universal nor gate this can be replaced by NOT function followed by AND function)because the CMOS and/or FPGA architectures consist of this structures really we can't known the structures how they are forming but they can turn to perform the operation. as a NOR gate, due to which the delay required will be reduced ,by the why it need less power. In this work, we present a technique that also aims at producing only $\frac{n}{2}$ rows, but by relying on a different approach than [10].

4 BASIC IDEA

The case of n _ n square multipliers is quite common, as the case of n that is a power of two. Thus, we start by focusing our attention on square multipliers, and then present the extension to the general case of m × n rectangular multipliers.

4.1 Square Multipliers

The proposed approach is general and, for the sake of clarity, will be explained through the practical case of 8 × 8 multiplication (as in the previous figures). As briefly outlined in the previous sections, the main goal of our approach is to produce a partial product array with a maximum height of $\frac{n}{2}$ rows, without introducing any additional delay.

Let us consider, as the starting point, the form of the simplified array as reported in Fig. 2, for all the partial product rows except the first one. As depicted in Fig. 6a, the first row is temporarily considered as being split into two sub rows, the first one containing the partial product bits (from right to left) from pp00 to pp80 and the second one with two bits set at "one" in positions 9 and 8. Then, the bit neg3 related to the fourth partial product row, is moved to become a part of the second sub row.

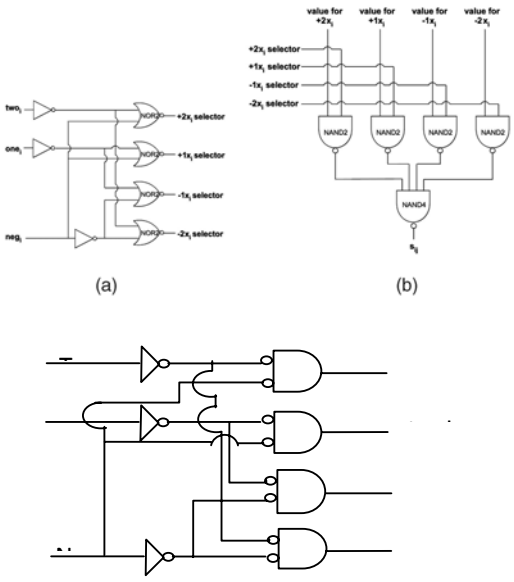


Fig. 4. Gate-level diagram for the generation of two's complement partial product rows [10]. (a) 3-5 decoder. (b) 4-1 multiplexer (c) proposed

Here ,when we are performing the sum peration on partial products from lower significant to higher significant position ,in this case we should maintain a consistent power for all partial products, and this is a time consuming process .instead of going

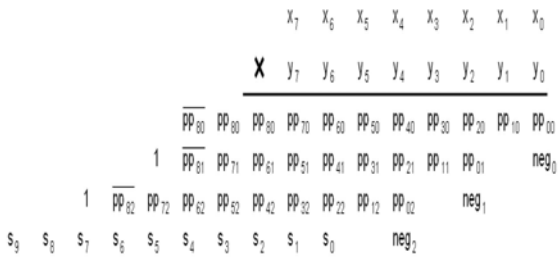


Fig. 5. Partial product array by applying the two's complement computation method in [10]

to the last row. through like this we should segregate the sequence in to two parts thereby we can reduce the power requirement from the hardware point of view we can realize this by NOT gate (enable).

The key point of this "graphical" transformation is that the second sub row containing also the bit neg3, can now be easily added to the first sub row, with a constant short carry propagation of three positions (further denoted as "3-bits addition"), a value which is easily shown to be general, i.e., independent of the length of the operands, for square multipliers. In fact, with reference to the notation of Fig. 6, we have that

(~qq90) qq90 qq80 qq70 qq60 = 0 0(~ pp80) pp70 pp60+ 0 1 1 0 neg3. As introduced above, due to the particular value of the second operand, i.e., 0 1 1 0 neg3, in [12], we have observed that it requires a carry propagation only across the least-significant three positions, a fact that can also be seen by the implementation shown in Fig. 7.

It is worth observing that, in order not to have delay penalizations, it is necessary that the generation of the other rows is done in parallel with the generation of the first row cascaded by the computation of the bits qq90 qq90 qq80 qq70 qq60 in Fig. 6b. In order to achieve this, we must simplify and differentiate the generation of the first row with respect to the other rows. We observe that the Booth recoding for the first row is computed more easily than for the other rows, because the y_1 bit used by the MBE is always equal to zero. In order to have a preliminary. Analysis which is possibly independent of technological details, we refer to the circuits in the following figures:

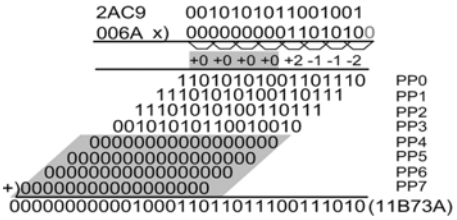


Fig. 6 Illustration of multiplication using modified Booth encoding

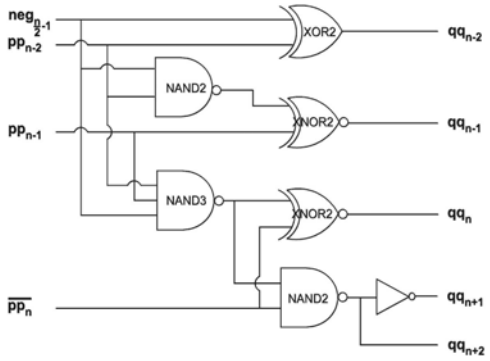


Fig. 7. Gate-level diagram of the proposed method for adding the last neg bit in the first row.

Which is possibly independent of technological details, we refer to the circuits in the following figures:

. Fig. 1, slightly adapted from [10, Fig. 12], for the partial product generation using MBE;

Fig. 7, obtained through manual synthesis (aimed at modularity and area reduction without compromising the delay), for the addition of the last neg bit to the three most significant bits of the first row;

. Fig. 8, obtained by simplifying Fig. 1 (since, in the first row, it is y2i_1=0), for the partial product generation of the first row only using MBE; and

. Fig. 9, obtained through manual synthesis of a combination of the two parts of Fig. 8 and aimed at decreasing the delay of Fig. 8 with no or very small area increase, for the partial product generation of the first row only using MBE.

In particular, we observe that, by direct comparison of Figs. 1 and 8, the generation of the MBE signals for the first row is simpler, and theoretically allows for the saving of the delay of oneNAND3gate. In addition, the implementation in Fig. 9 has a delay that is smaller than the two parts of Fig. 8, although it could require a small amount of additional area. As we see in the following, this issue hardly has any significant impact on the overall design, since this extra hardware is used only for the three most significant bits of the first row, and not for all the other bits of the array.

The high-level description of our idea is as follows:

1. generation of the three most significant bit weights

of the first row, plus addition of the last neg bit:

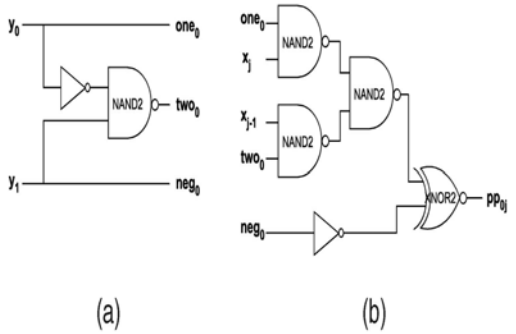


Fig. 8. Gate-level diagram for first row partial product generation. (a) MBE signals generation. (b) Partial product generation.

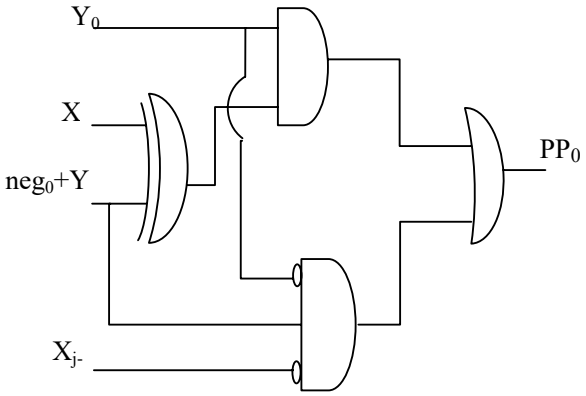


Fig. 9. Combined MBE signals and partial product generation for the first row (improved for speed).

.possible implementations can use a replication of three times the circuit of Fig. 9 (each for the three ost significant bits of the first row), cascaded by the ircuit of Fig. 7 to add the neg signal;

2. Parallel generation of the other bits of the first row. Possible implementations can use instances of the circuitry depicted in Fig. 8, for each bit of the first row, except for the three most significant;

3. Parallel generation of the bits of the other rows possible implementations can use the circuitry of Fig. 1, replicated for each bit of the other rows. All items 1 to 3 are independent, and therefore can be executed in parallel. Clearly if, as assumed and expected,

Item 1 is not the bottleneck (i.e., the critical path), then the implementation of the

in parallel. Clearly if, as assumed and expected, item 1 is not the bottleneck (i.e., the critical path), then the implementation of the proposed idea as reached the goal of not introducing time penalties.

TABLE 2

Design of the generation of the PP rows Considered in the evaluation

Implementation	Description	Motivation
Standard multiplier (Any row)	Standard implementation of the MBE: signals *one*, *two*, and *neg* generated first, and then used to produce the partial product array (Fig. 1).	The delay to generate a generic partial product row (other than the first one) in a standard $n \times n$ multiplier represents the upper bound for any design aimed at removing the last *neg* signal (either working on the first or last row).
Standard multiplier (First row)	Alternative implementation of the MBE for the first row: logic for the generation of the partial product row is simplified as the y_{-1} bit is always equal to zero (Fig. 8).	The delay to produce the first row consitutes the lower bound for any scheme trying to get rid of the MBE negative encoding by incorporating its effect in the first row, as in the proposed method.
Proposed method	Generation of the first partial product row and fast 3-bit carry-propagate addition (Fig. 6).	The aim is to reduce the number of partial product rows from $\lceil n/2 \rceil + 1$ to $\lceil n/2 \rceil$, thus getting rid of the effect of MBE negative encoding. By having fewer partial product rows, the next reduction hardware can be smaller in size and faster in speed. The delay will be higher than the one for the first row for a standard multiplier, but it should be lower than any of the other PP rows, thus not inducing any time penalty.
Two's complement	Direct computation of the last partial product row in two's complement performed in parallel with the production of the partial products of the other rows (using the designs in Fig.s 3 and 4, as in [9].	Similarly to the method proposed above, this scheme avoids the extra partial product row, and its delay has to be within the delay requirements of the standard PP rows. The above goal is achieved by replacing the partial product generation on the last row with partial product selection of the multiplicand's two's complement, thus eliminating the need for the last *neg* signal.

4.2 **Segregation of Rectangular Multipliers by SPST technique**

A number of potential product extensions to the proposed method exist, including rectangular multipliers, higher radix MBE, and multipliers with fused accumulation [12]. Here, we quickly focus on m _ n rectangular multipliers. With no loss of generality, we assume m × n, i.e., m = n +m' with m0≥ 0,. Here if we used a technique called spurious power suppuration technique(SPST),we are going to reduce power requirement, to half of the power which require in rectangular (basic) partial product summation. Since it leads to a smaller number of rows; for simplicity, and also with no loss of generality, in the following, we assume that both m and n are even. Now, we have seen in Fig. 6a, that for m0'= 0 then the last neg bit, i.e., $neg_{n/2\_1}$ belongs to the same column as the first row partial product $pp_{n/2};0$. We find that the first partial product row has bits up to $(\sim pp_{m,}0)$; therefore, in order to also include in the first row the contribution of $neg_{n/2\_1}$, due to the particular nature of operands it is require to perform a (m'+ 3)-bit carry propagation (i.e., a (m'+ 3)bit addition) in the sum $(\sim qq_{m+1,}0)qq_{m+1,}0qqm,0 \ldots qqn\_2;0 = 00(\sim pp_{m},0) \ldots pp_{n-2,0} +0\ 1\ 1 \ldots 0\ neg_{n/2\text{-}1}$. Thus, for rectangular multipliers, the proposed approach can be applied with the cost of a (m'+ 3)-bit addition. The complete or even partial execution overlap of the first row with other rows generation clearly depends on a number of factors, including the value of m0 and the way that the (m'+ 3)-bit addition is implemented, but still the proposed approach offers an interesting alternative that can possibly be explored for designing and implementing rectangular multipliers.

5.EVALUATIONAND COMPARISONS

In this section, the proposed method based on the addition of the last neg signal to the first row is first evaluated. The designed architecture is then compared with an implementation based on the computation of the two's complement of the last row (referred to as "Two's complement" method) using the designs for the 3-5 decoders, 4-1 multiplexers, and two's complement tree in [10]. Moreover, in the analysis, the standard MBE implementations for the first and for a generic partial product row are also taken into account (as

Summarized in Table 2).

For all the implementations, we explicitly evaluate the most common case of a n × n multiplier, although we have shown in Section 4 that the proposed approach can also be extended to m _ rectangular multipliers. While studying the framework of possible implementations, we considered the first phase of the multiplication algorithm (i.e., the partial product generation) and we focused our attention on the issues of area occupancy and modular design, since it is reasonable to expect that they lead to a possibly small multiplier with regular layout. The detailed results of some extensive evaluations and comparisons, both based on theoretical analysis and related implementations are reported in [12].

TABLE 3

Gate Delay and Area Cost Normalized to the Delay of One INV Gate with a Load of Four and to the Area of a NAND2 Gate

(ST Microelectronics 130nm HCMOS Technology)

Gate	Normalized gate delay	Normalized area cost	Function
INV	1.00	0.75	1-input inverter
NAND2	1.35	1.00	2-input NAND
NAND3	1.90	1.25	3-input NAND
NAND4	2.75	1.25	4-input NAND
NOR2	1.85	1.00	2-input NOR
XNOR2	2.75	2.00	2-input XNOR
XOR2	3.15	2.00	2-input XOR

1. Theoretical analysis based on the concept of equivalent gates from Ganske's analysis [22] (as in [10]),

2. Theoretical analysis based on delay and area costs for elementary gates in a standard cell library,

3. Theoretical analysis showing that the proposed approach, in the version minimizing area, can very likely overlap the generation of the first row with the generation of the other rows, and

4. Validation by logic synthesis and technology mapping to an industrial cell library. All the results show the feasibility of the proposed approach. Here, for the sake of simplicity, we quickly summarize the results of the theoretical analysis and we check the validity of our estimations through logic synthesis and simulation

. **5**.*1 High-Level Remarks and theoretical*

Calculations

Analysis As can be seen from Fig. 6, the generation of the first row is different from the generation of the other rows, basically for two reasons: . the first row needs to assimilate the last neg signal, an operation which requires an addition over the three most significant bit weights; the first row can take advantage of a simpler Booth recoding, as the y-1 bit used by the BE is always equal to zero (Section 4). As seen before, in Fig. 8, we have a possible implementation to generate the first row, which takes into account the simpler generation of the MBE signals. We have seen that by combining the two parts of Fig. 8 we get Fig. 9, which is faster than Fig. 8, at a possibly slightly larger area cost certainly very marginal with respect to the global area of all the partial product bits coming from the other rows. We have done some rough simulations and found that a good trade-off could be to have the generation of the first bits of the first row carried out by the circuit of Fig. 9, followed by the cascaded addition provided by Fig. 7 (Section 4). Based on all of the above, our architecture has been designed to perform the following operations:

1. generation of the three most significant bit weights of the first row (through the very small and regular circuitry of Fig. 9) and addition to these bits of the neg signal (by means of the circuitry of Fig. 7);

2. Generation of the other bits of the first row, using the circuitry depicted in Fig. 8; and

3. Generation of the bits of the other rows, using the circuitry of Fig. 1. As these three operations can be carried out in parallel, the overall critical path of the proposed architecture emerges from the largest delay among the above paths. Critical path and area cost for the proposed architecture, as well as for the other implementations in Table 2, were computed with reference to a 130 nm HCMOS standard cell

Table:4 Delay comparison over the Hard ware

Technique	Part	8x8	16x16	32x32
Standard Multiplier delay	3-5 decoder	10.40	10.40	10.40
	Combined MBE&PP generation	11.60	11.60	11.60
	T0tal	22	22	22
Proposed method delay	3-5 decoder	8.40	8.40	8.40
	Combined MBE&PP generation	7.85	7.85	7.85
	T0tal	16.25	16.25	16.25

library from STMicroelectronics [23] (later used also for obtaining overall synthesis results). In this analysis, the contribution of wires was neglected, and a buffer-free configuration was considered. Nonetheless, details regarding buffer stages location and size are discussed in [12]. Data concerning area and delay for elementary cells used in this work (as well as in [9]) parented. It is worth observing that results may vary depending on specific parameters elected for the synthesis such as logic implementation, optimization strategies', and target libraries. We observe that the "Two's Complement" approach has a delay that is longer than the delay to generate the standard partial product rows, becoming even

longer as the size n of the multiplier increases (e.g., exceeding the delay of a XNOR2 gate starting from (n = 16). On the other hand, according to theoretical estimations, we can see that the delay for generating the first row in the proposed method estimated to be lower than the delay for generating the standard rows.

This means that the extra row is eliminated without any penalty on the overall critical path. With respect to area costs, it can be observed that the proposed method hardly introduces any area overhead with respect to the standard generation of a partial product row. On the other hand, the "Two's Complement" approach requires additional hardware, which increases with the size

Table -5: Estimated hardware cost for the implementation

Technique	part	8X8	16X16	32X32
Standard Multiplier	Generating MBE signal	11	11	11
	Generating PP	52	98	190
	Total	63	109	201
Proposed method	Generating MBE signal	2	2	2
	Generating PP	52	98	190
	3-5 decoder	2.75	2.75	2.75
	Combined MBE&PP generation	3.75	3.75	3.75
	T0tal	60.50	60.5	60.50

6 CONCLUSIONS

Two's complement n ×n multipliers using radix-4 Modified Booth Encoding produce $\frac{n}{2}$ partial products but due to the sign handling, the partial product array has a maximum height of $\frac{n}{2}+1$. We presented a scheme that produces a partial product array with a maximum height of $\frac{n}{2}+1$, without introducing any extra delay in the partial product generation stage. With the extra hardware of a (short) 4-bit addition, and the simpler generation of the first partial product row, we have been able to achieve a delay for the proposed scheme within the bound of the delay of a standard partial product row generation. As well if we SPSPT technique ,we can reduce the power requirement to half as. The outcome of the above is that the reduction of the maximum height of the partial product array by one unit may simplify the partial product reduction

tree, both in terms of delay and regularity of the layout. This is of special interest for all multipliers, and especially for single-cycle short bit-width multipliers for high performance embedded cores, where short bit-width multiplications are common operations. We have also compared our approach with a recent proposal with the same aim, considering results using a widely used industrial synthesis tool and a modern industrial technology library, and concluded that our approach may improve both the performance and area requirements of square ultiplier designs. The proposed approach also applies with minor modifications to rectangular and to general radix-B Modified Booth Encoding multipliers.

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AUTHENTICATED GROUP KEY TRANSFER PROTOCOL USING NOVEL APPROACH

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Qiscet,Ongole.

Abstract—Group key transfer protocol is developed to establish the communication path for group of communicating entities. TheKey transfer protocols rely on a mutually trusted key generation center (KGC) to select session keys and transport session keys to all communication entities secretly. Most often, KGC encrypts session keys under another secret key shared with each entity during registration. In this paper we propose a key transfer protocol for secure communication between group of users in a wireless networks. Here we state an authenticated key transfer protocol based on secret sharing scheme that KGC can broadcast group key information to all group members at once and only authorized group members can recover the group key; but unauthorized users cannot recover the group key. We also provide authentication for transporting this group key and the confidentiality of this transformation is information theoretically secure.

This approach requires that a trusted sever be set up, and it incurs communication overhead costs. In addition, the existing group key transfer protocols based on secret sharing all use threshold schemes that need to compute a t -degree interpolating polynomial to encrypt and decrypt the secret group key, then it increases the computational complexity of system. In this paper, we first present a novel group key transfer protocol without an online KGC, which is based on DH key agreement and a perfect linear secret sharing scheme (LSSS). The confidentiality of the group key transfer phase of this protocol is information theoretically secure, which is ensured by this LSSS. Furthermore, this protocol can resist potential attacks and also reduce the overhead of system implementation.

I. INTRODUCTION

In order to ensure secure communication, before exchanging communication messages, a key establishment protocol will distribute one-time secret session keys to all participants, which needs to provide confidentiality and authentication for session keys.
Namely, confidentiality ensures the sender that the message can be read only by an intended receiver and authentication ensures the receiver that the message was sent by a specified sender and the message was not altered en route

There are other distributed group key management protocols based on non-DH key agreement approach. Tzengproposed conference key agreement protocol based on discrete logarithm (DL) assumption with fault tolerance in recent years. The protocol can establish a conference key even if there are several malicious participants among the conference participants. However, the protocol requires each participant to create n-power polynomials, where n is the number of participants; this is a serious encumbrance to efficiency. In 2008, Cheng and Lain modified Tseng'sconference key agreement protocol based on bilinear pairing. In 2009, Huang e proposed a no interactive protocol based nodal assumption to improve the efficiency of Tseng's protocol. One main concern of key agreement protocols is that since all communication entities are involved to determine session keys, the time delay of setting up this group key may be too long, especially when there are a large number of group members.

Since avoiding the use of encryption one by one can introduce less computation complexity, secret sharing has been used to design group key distribution protocols, which was first introduced by both Blakely [1] and Shamir [29] independently in 1979. There are two different approaches using secret sharing: one assumes a trusted offline server active only at initialization [4], [15], [28], [3] and the other assumes an online trusted server, called the key generation center (KGC), always active. The first type of approach is also called the key redistribution scheme. The main disadvantage of this approach is to require every user to store a large size of secrets. The second type of approach requires an online server to be active [24]. It is similar to the model used in the IEEE 802.11i standard [20]. In 1989, Laih et al. [24] proposed the first algorithm based on this approach

using any (t, n) secret sharing scheme to istribute a group key to a group consisting of (t −1)

Later, there are some papers [2], [25], [28] following the same concept to propose ways to distribute group messages to multiple users. Recently, [18] proposed a group key transfer protocol using (t, n) secret sharing that provided confidentiality and authentication, where KGC and each group member need to compute a t -degree interpolating polynomial to encrypt and decrypt the secret group key respectively. Then [26]

pointed out that [18] could not protect users' long-term secrets against a malicious user and further gave an improvement. The main disadvantage of the approach of relying on an online KGC is that the trusted KGC is required in distributing the group key and it increases the overhead of system.

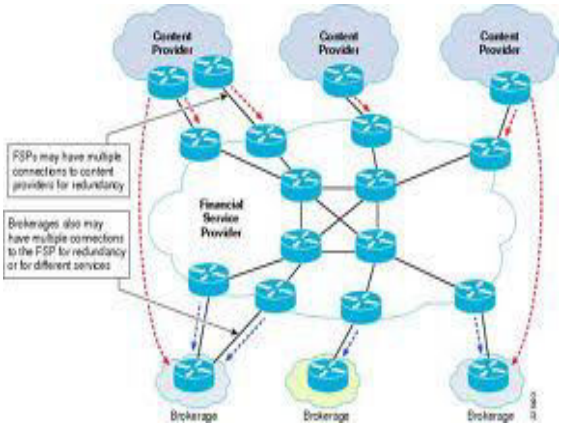
Secret sharing has been used to design group key distribution protocols. There are two different approaches using secret sharing: one assumes a trusted offline server active only at initialization and the other assumes an online trusted server, called the key generation center, always active. The first type of approach is also called the key predistribution scheme. In a key predistribution scheme, a trusted authority generates and distributes secret pieces of information to all users offline. At the beginning of a conference, users belonging to a privileged subset can compute individually a secret key common to this subset. A family of forbidden subsets of users must have no information about the value of the secret. The main disadvantage of this approach is to require every user to store a large size of secrets. The second type of approach requires an online server to be active and this approach is similar to the model used in the IEEE 802.11i standard that employs an online server to select a group key and transport it to each group member. However, the difference between this approach and the IEEE 802.11i is that, instead of encrypting the group temporal key (GTK) using the key encryption key (KEK) from the authentication server to each mobile client separately as specified in the IEEE 8-2.11i, the trusted KGC broadcasts group key information to all group members at once. In 1989, Laih proposed the first algorithm based on this approach using any secret sharing scheme to distribute a group key.

In this paper, we first adopt the advantages of DH key agreement and LSSS to design a secure and efficient key transfer protocol without an online KGC. The confidentiality of the group key transfer phase of this protocol is information theoretically secure, which is ensured by a perfect LSSS. We classify attacks into insider and outsider attacks separately, and analyze our protocol under these attacks in detail.

Device pairing has recently attracted a significant amount of interest from the research community, fueled by the pro-liberation of wireless mobile devices. Prior work addresses similar key exchanges, but either assumes a public key infrastructure [6,8,23,24,41,42,44], cumbersome key-exchange protocols [5], is vulnerable to malicious bystanders [2], or are restricted to two-party exchanges [3,7,9,27,30,32,38–40,45]. Other works over's mechanisms optimized for large groups of 10 to 30 people [10]. This work focuses on small groups where users can accurately count the group size [25]: eight or fewer. Assuming group size fits a Zipf distribution, the majority of groups will be within the range covered by the NOVEL AGK protocol

II. SYSTEM ARCHITECTURE

The following figure describes the architecture of system. Here every user needs to establish a connection with other user in the network to communicate with each other. This is done by sending request to the kernel for new channel. To start a connection initially each user must be register with the key generation centre (KGC).The KGC is used to generate the private keys to each user. Using these keys KGC will generate the session key for encryption and decryption. Here every member must register with the KGC to start the connection; KGC generates session keys using all user keys. These session keys are passed to all users to establish the connection. The KGC will forward the session key to end user these session keys are encrypted and decrypted by using secrete key to achieve the confidentiality and security.



III. KEY DISTRIBUTION SCHEMA

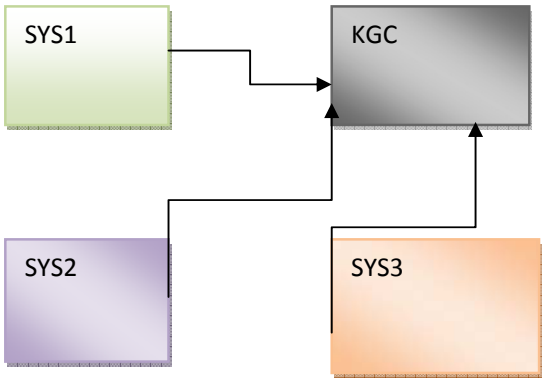
Group key generation and distribution: Upon receiving a group key generation request from any user, KGC needs to randomly selects a group key and access all shared secrets with group members. KGC needs to distribute this group key to all group members in a secure and authenticated manner. All communication between KGC and group members is in a broadcast channel

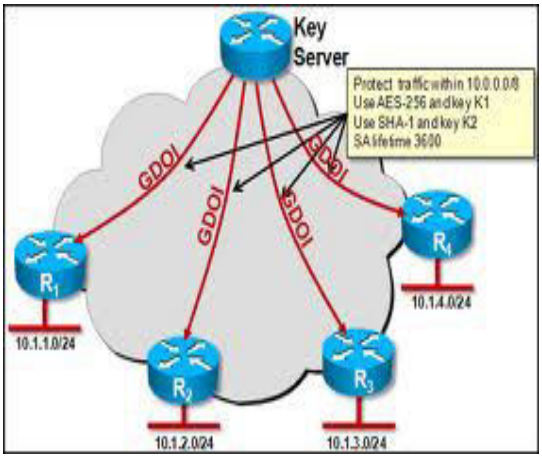
Suppose that S is the secret-domain and Pi is the share-domain of participant i , Where $1 \leq i \leq n$. When a dealer D wants to share a secret s Samong a set of Participants P i ,i={1... n}, he will give each participant a share si.

Isolated links do not carry any traffic. Restricted links are used to isolate nodes from traffic forwarding. The restricted link weight wr must be set to a sufficiently high, finite value to achieve that.

Nodes are isolated by assigning at least the restricted link weight to all their attached links.

For a node to be reachable, we cannot isolate all links attached to the node in the same configuration. More than one node may be isolated in a configuration. The set of isolated nodes in Ci is denoted Si, and the set of normal (non-isolated) nodes Si = N \ Si.





IV. SECURITY GOALS

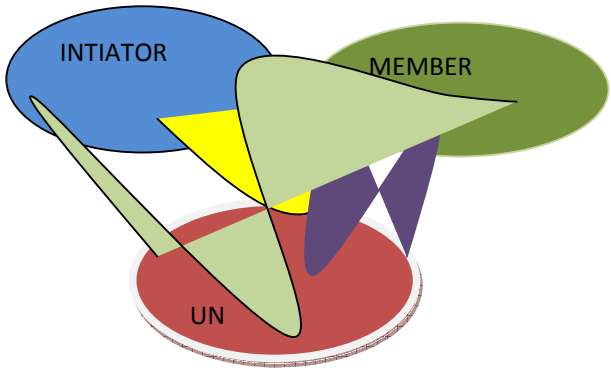
Proof. In order to transfer the group key, the initiator randomly selects a group keyKG and makes n −1 values, U i €(K G − Ki) mod p for i €1,..., n −1 ,publicly known.For each authorized group member, with knowledge of the one-time secret shared with the initiator and the public information, he/she knows Ui and is able to compute the inner product (yi v(xi), r) € Ki . Thus, any authorized group member is able to reconstruct the group key K G€ (U i U Ki) od p , where the vector r €(ri ,..., rn) € K n . However, the one-time secret (xi|| yi) € si of ach group member shared with the initiator cannot be traced by outsiders.

For an insider j , he/she knows the group key and Ui , then he can obtain Ki from K G € (U i U Ki) mod p . However, j cannot solve the secret (xi || yi) € si from the equation (yi v(xi), r) € Ki since there are two unknown quantities. At the same time, due to the fact the secret (xi || yi) || siof each group member shared with the initiator depends on the random numbers (ri , rn)and long-term private keys(prk i , prkn) , the one-time secret si is still untraceable by insiders. Termination

The algorithm runs through nodes trying to make them isolated in one of the backup configurations always terminate with or without success.

If a node cannot be isolated in any of the configurations, the algorithm terminates without success. However, the algorithm is designed so that any bi-connected topology will result in a successful termination, if the number of configurations allowed sufficiently high.

Remark 2. Most key transfer schemes based on TSSS are claimed information theoretically secure. However, these schemes must pre-share secrets (shadows) between the dealer and the participants. It means that the secrets must be shared via a secure channel. Actually, it is a strong assumption to suppose that a secure channel is existed in public networks. That is, most existing schemes do not propose any practical method to share secrets in public networks. In this paper, we first used the CDH assumption to share the secrets between the initiator and other participants. Next, we construct a group key transfer protocol based on a perfect LSSS, which is no need to compute a t -degree interpolating polynomial to encrypt and decrypt the group key. This LSSS is information theoretically secure since there has no other computational assumption based upon. Hence, we say that the group key.



ADVANTAGES

Each user needs to register at KGC to subscribe the group key transfer service and to establish a secret with KGC. Thus, a secure channel is needed initially to share this secret with each user. Later, KGC can transport the group key and interact with all group members in a broadcast channel. The confidentiality of group key distribution is information theoretically secure; that is; the security of this transfer of group key to each group member does not depend on any computational assumption. The authentication of the group key is achieved by broadcasting a single authentication message to all group members.

CONCLUSIONS

We have proposed an efficient group key transfer protocol based on secret sharing. Every user needs to register at a trusted KGC initially and preshare a secret with KGC. KGC broadcasts group key information to all group members at once. The confidentiality of our group key distribution is information theoretically secure. We provide group key authentication. Security analysis for possible attacks is included.

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TOWARDS ENSURING SECURITY IN DATA MANAGEMENT IN CLOUD COMPUTING

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Abstract:-Cloud computing is the use of computing resources (hardware and software) that are delivered as a service over a network. Cloud computing is a model for enabling convenient, on demand network access to a shared pool of configurable computing resources that can be rapidly provisioned and released with minimal management effort or service provider interaction. However along with these advantages, storing a large amount of data including critical information on the cloud motivates highly skilled hackers thus creating a need for the security to be considered as one of the top issues while considering Cloud Computing. In this paper we explain the cloud computing along with its open secure architecture advantages in brief and emphasize on various security threats in cloud computing also the existing methods to control them along with their pros and cons.

1. INTRODUCTION

Cloud computing is emerging technology in today's world of virtualization. Before cloud computing is only used in business ideas as support to growing demand in services in cloud computing. Now a days everyone can use cloud computing freely and as well as paid usage as the only deference is the security of the data in cloud computing.

What is cloud computing? Cloud computing offers different services such as Infrastructure as a Service (IaaS), Platform as a Service (PaaS) and Software as a Service (SaaS). These services are offered by different servers placed at different part of the world. So there will be clouds of servers doing the services at different location. So this is called cloud computing. Data should be sent from one server to different server for processing in cloud. These data should be controlled and managed to prevent unauthorized access to the data in the processing the cloud as well as the accessed by the client or end users. Cloud computing environment is generally assumed as a potential cost saver as well as provider of higher service quality. Security, Availability, and Reliability are the major quality concerns of cloud service users. Gens et. al. [10], suggests that security in one of the prominent challenge among all other quality challenges.

In a virtualized environment where infrastructure is shared across multiple tenants, your data is commingled with that of other customers at every phase of the life cycle—during transit, processing, and storage. Hence, it is important to understand the location of the service, service-level guarantees such as inter-node communication, and storage access (read and write) latency.

1.1 Characteristics of cloud computing

Cloud computing exhibit five essential characteristics defined by NIST (National Institute of Standards and Technology) [1].

1. On-demand self-service. A consumer can unilaterally provision computing capabilities.
2. Broad network access. Capabilities are available over the network and accessed through standard mechanisms that promote use by heterogeneous thin or thick client platforms.
3. Resource pooling. The provider's computing resources are pooled to serve multiple consumers, with different physical and virtual resources dynamically assigned and reassigned according to consumer demand.
4. Rapid elasticity. Capabilities can be rapidly and elastically provisioned, in some cases automatically, to quickly scale out and rapidly released to quickly scale in.
5. Measured service. Cloud systems automatically control and optimize resource use by leveraging a metering capability at some level of abstraction appropriate to the type of service.

1.2 Security Benefits Of Cloud Computing

Current cloud service providers operate very large systems. They have sophisticated processes and expert personnel for maintaining their systems, which small enterprises may not have access. [4] As a result, there are many direct and indirect security advantages for the cloud users. Here we present some of the key security advantages of a cloud computing environment:

Data Centralization: In a cloud environment, the service provider takes care of storage issues and small business need not spend a lot of money on physical

storage devices. Also, cloud based storage provides a way to centralize the data faster and potentially cheaper. This is particularly useful for small businesses, which cannot spend additional money on security professionals to monitor the data.

Incident Response: IaaS providers can put up a dedicated forensic server that can be used on demand basis. Whenever a security violation takes place, the server can be brought online. In some investigation cases, a backup of the environment can be easily made and put onto the cloud without affecting the normal course of business.

Forensic Image Verification Time: Some cloud storage implementations expose a cryptographic check sum or hash. For example, Amazon S3 generates MD5 (Message Digest algorithm 5) hash automatically when you store an object [10]. Therefore in theory, the need to generate time consuming MD5 checksums using external tools is eliminated.

Major drawback of cloud computing is its transparency, that is end-user or client does not know how and where the data is processing or it is storing. Depending on the country in which data is stored the legal terms are different and there is no guarantee that the data is really secure in the cloud computing.

1.3 Security Disadvantages in Cloud Environments [5]

Data Location: In general, cloud users are not aware of the exact location of the datacenter and also they do not have any control over the physical access mechanisms to that data. Most well-known cloud service providers have datacenters around the globe. Some service providers also take advantage of their global datacenters. However, in some cases applications and data might be stored in countries, which can judiciary concerns.

Investigation: Investigating an illegitimate activity may be impossible in cloud environments. Cloud services are especially hard to investigate, because data for multiple customers may be co-located and may also be spread across multiple datacenters. Users have little knowledge about the network topology of the underlying environment. Service provider may also impose restrictions on the network security of the service users.

Data Segregation: Data in the cloud is typically in a shared environment together with data from other customers. Encryption cannot be assumed as the single solution for data segregation problems. In some situations, customers may not want to encrypt data because there may be a case when encryption accident can destroy the data.

Long-term Viability: Service providers must ensure the data safety in changing business situations such as mergers and acquisitions. Customers must ensure data availability in these situations. Service provider must also make sure data security in negative business conditions like prolonged outage etc.

Compromised Servers: In a cloud computing environment, users do not even have a choice of using physical acquisition toolkit. In a situation, where a server is compromised; they need to shut their servers down until they get a previous backup of the data. This will further cause availability concerns.

Regulatory Compliance: Traditional service providers are subjected to external audits and security certification. If a cloud service provider does not adhere to these security audits, then it leads to an obvious decrease in customer trust.

Recovery: Cloud service providers must ensure the data security in natural and man-made disasters. Generally, data is replicated across multiple sites. However, in the case of any such unwanted event, provider must do a complete and quick restoration.

This paper deals with various survey in data management in cloud computing and optimized solution. Our survey deals with solution of auditing, accounting and logging mechanism in the cloud computing.

2. LITERATURE SURVEY

2.1 Mirage Image Management System [10]

The security and integrity of VM images are the foundation for the overall security of the cloud since many of them are designed to be shared by different and often unrelated users. This system addresses the issues related to secure management of the virtual-machine images that encapsulate each application of the cloud.

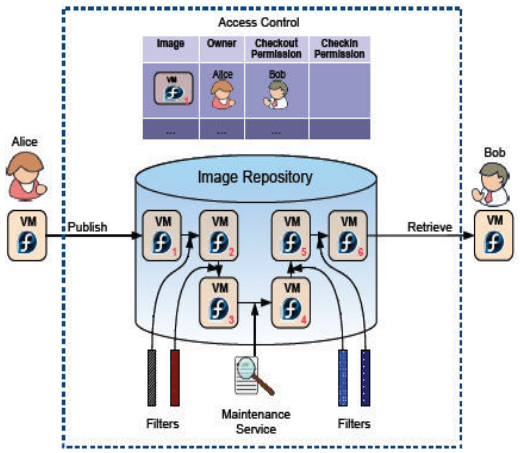

Figure 1: Security Features of the Mirage Image Management System

Figure 1 shows the overall architecture of Mirage Image Management System.
Mirage Image Management System consists of 4 major components:
1. **Access Control**. This framework regulates the sharing of VM images. Each image in the repository has a unique owner, who can share images with trusted parties by granting access permissions.
2. **Image Transformation by Running Filters.** Filters remove unwanted information from images at publishes and retrieval time. Filters at publish time can remove or hide sensitive information from the publisher's original image. Filters at retrieval time filters may be specified by the publisher or the retriever.
3. **Provenance Tracking.** This mechanism that tracks the derivation history of an image.
4. **Image maintenance**. Repository maintenance services, such as periodic virus scanning, that detect and fix vulnerabilities discovered after images are published.

Advantages. Filters mitigate the risk in a systematic and efficient way. The system stores all the revisions which allows the user to go back to the previous version if the
current version if she desires. The default access permission for an image is private so that only owner and system administrator can access the image and hence untrusted parties cannot access the image.

Limitations. Huge performance overheads, both in space and time. Filters cannot be 100% accurate and hence the system does not eliminate risk entirely. Virus scanning does not guarantee to find all malware in an image. "The ability to monitor or control customer content" might increase the liability of the repository provider

2.2 Client Based Privacy Manager[11]

Client based privacy manager helps to reduce the risk of data leakage and loss of privacy of the sensitive data processed in the cloud, and provides additional privacy related benefits.

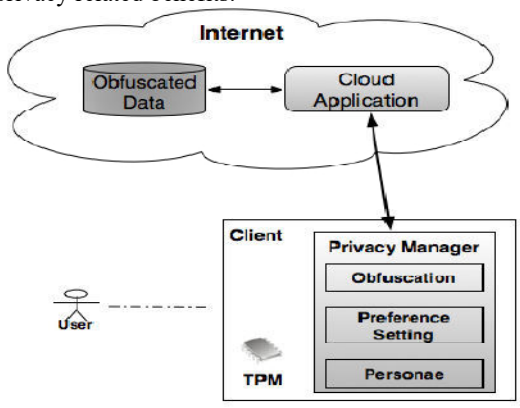

Figure 2. Client-Based Privacy Manager

Figure 2 shows the overall architecture of the privacy manager. The main features of the privacy manager are:

Obfuscation. This feature can automatically obfuscate some or all of the fields in a data structure before it is sent off to the cloud for processing, and translate the output from the cloud back into de-obfuscated form. The obfuscation and de-obfuscation is done using a key which is chosen by the user and not revealed to cloud service providers.
Preference Setting. This is a method for allowing users to set their preferences about the handling of personal data that is stored in an unobfuscated form within the cloud. This feature allows the user greater control over the usage of his data.
Data Access. The Privacy Manager contains a module that allows users to access personal information in the cloud, in order to see what is being held about them, and to check its accuracy. This is an auditing mechanism which will detect privacy violations once they have happened.
Feedback. The Feedback module manages and displays feedback to the user regarding usage of his personal information, including notification of data usage in the cloud. This module could monitor personal data that is transferred from the platform.
Personae. This feature allows the user to choose between multiple personae when interacting with cloud services.

Advantages. This solution solves many practical problems such as Sales Force Automation Problem, Customized End-User Services Problem and Share Portfolio Calculation problem.

Disadvantages. If the service provider does not provide full cooperation the features of the Privacy Manager other than obfuscation will not be effective, since they require the honest cooperation of the service provider. The ability to use obfuscation without any cooperation from the service provider depends not only on the user having sufficient computing resources to carry out the obfuscation and deobfuscation, but also on the application having been implemented in such a way that it will work with obfuscation.

2.3 Transparent Cloud Protection System (TCPS) [11]

TCPS is a protection system for clouds aimed at transparently monitoring the integrity of cloud components. TCPS is intended to protect the integrity of guest Virtual Machines (VM) and of the distributed computing middleware by allowing the host to monitor guest VMs and infrastructure components.

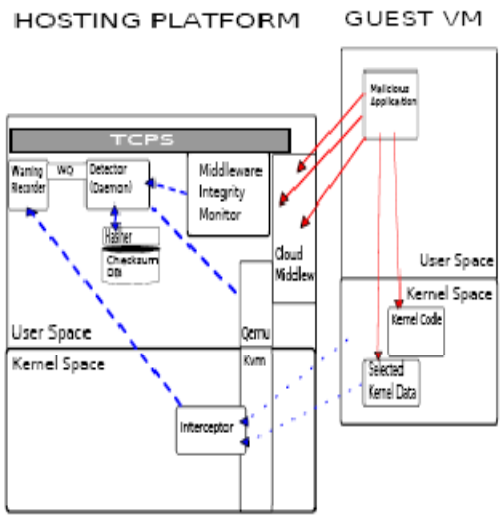

Figure 3: TCP Architecture.

Figure 3 shows the architecture of TCPS. TCPS is a middleware whose core is located between the Kernel and the virtualization layer.

By either actively or passively monitoring key kernel or cloud components
TCPS can detect any possible modification to kernel data and code, thus guaranteeing that kernel and cloud middleware integrity has not been compromised and consequently no attacker has made its way into the system.
The high level TCPS architecture is depicted in Figure 3, where potentially dangerous data flows are depicted in continuous lines and monitoring data flows are depicted in dashed lines. All TCPS modules reside on the Host and Qemu is leveraged to access the guest. Suspicious guest activity can be noticed by the Interceptor and they are recorded by the Warning Recorder into the Warning Queue where the potential alteration will be evaluated by the Detector component. TCPS can locally react to security breaches or notify the distributed computing security components of such an occurrence.

Advantages. This system is effective in detecting most kind of attacks. This system is able to avoid false-positives (Guest maintenance tolerance). The system minimizes the visibility from the VMs (Transparency). The system and the sibling guests are protected from attacks of a compromised guest. The system can be deployed on majority of the available middleware. The system can detect an intrusion attempt over a guest and, if required by the security policy, takes appropriate actions against the attempt or against the compromised guest and/or notify remote middleware security-management components.

2.4 Secure and Efficient Access to Outsourced Data [12]

Providing secure and efficient access to outsourced data is an important component of cloud computing and forms the foundation for information management and other operations.

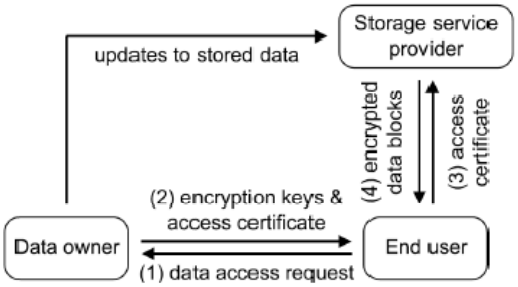

Figure 4: Illustration of application Scenario

Problem. Figure 4 shows the typical owner-write-user read scenario. Only the owner can make updates to the outsourced data, while the users can read the information according to access rights. Since the data owner stores a large amount of information on the untrusted service provider, the owner has to encrypt the outsourced data before putting on the server. The outsourced data will be accessed by different end users all over the network and hence computationally expensive operations on the data blocks (smallest unit of data) should be avoided and the amount of data stored in the end users must be reduced. Right keys should be provided to the end users to control their access.

Solution. Fine-grained access control should be provided for the outsourced data by encrypting every data block with a different symmetric key. Flexible and efficient management by adopting the key derivation method to reduce the number of secrets maintained. Data isolation among end users by adopt over-encryption and lazy revocation.

2.4.1 Data Access Procedure

1. (End user) sends a data access request to the data owner.
2. (Data owner) authenticate the sender, verify the request, and determine the smallest key set.
3. (End user) sends to the service provider.
4. (Service provider) verify the cert, check the user and ACM index, and retrieve data blocks and conduct the over-encryption.
5. (End user) receive the data blocks, use seed and K' to derive keys, and then recover the data.

Using conventional access control mechanisms, once the access rights are granted, the data will be fully available at the service provider.

2.4.2 Dynamics in Use Access Rights.

• **Grant Access Right.** The owner will change the access control matrix and increase the value of ACM index. The service provider and end user do not need to change to adapt to this update.

• **Revoke Access Right:** Depends on whether or not the service provider conducts over encryption. If the service provider conducts over encryption, the owner updates the access control matrix, increases the value of ACM index and sends this new ACM index to the service provider until it receives acknowledgement. If the services provider refuses to conduct over encryption, then adopt lazy revocation to prevent revoked users from getting access to updated data blocks.

2.4.3 Dynamics in Outsourced Data.

• **Block Deletion.** A special control block is used to replace the deleted block. The owner will label its access control matrix to show that the block no longer exists

• **Block Update.** The control block is encrypted with kp,I and write it to the i-th block of the outsourced data. The control block will contain the following information: (1) a pointer to the data block in which D| I is currently stored; (2) information used by the data owner to derive the encryption key of D| i ; (3) information used by the data owner to verify the integrity of the control block. The owner will also use the new secret to encrypt D0i and write it to the corresponding place in S.

• **Block Insertion and Appending.** The data owner will locate an unused block index, derive the encryption key in the hierarchy using k0,1, encrypt the data block, and store it on the service provider. The new data blocks are inserted based on their access patterns.

Advantages. Data access procedure reduces the overhead of the data owner and prevents the revoked users from getting access to the outsourced data. This approach is robust against collusive attacks if the hash function is safe. Over-encryption conducted by the service provider defends against eavesdroppers even when they have the data block encryption keys. This approach has less communication and overhead for data retrieval when they have infrequent update operations. This approach handles user revocation without impacting service provider.

Disadvantages. This approach is applicable only for owner-write-users-read applications and hence not generic. There is a lengthened data retrieval delay caused by the access to updated data blocks.

3. CONCLUSION

In today's modern world, innovation of modern technologies is becoming inevitable to satisfy the customer's requirements. To overcome the business demands, the company has to keep an eye on worldwide collaboration, innovation and productivity [7]. These are the essentials for a company to compete with other companies. Thus the concept cloud computing evolves. In this paper there are papers related to security in data management in cloud computing. Each paper deals with security and solving particular issues. Still cloud computing is emerging as important field in mass storage, and other infrastructure facilities because of its advantages. However cloud computing is still in its infancy, with positive and negative comments made on its possible implementation for a large-sized enterprise.

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CONFIDENCE AND SECURITY IN ONLINE TRANSACTION: AN E-COMMERCE PERSPECTIVE

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Abstract—Confidence is the key to the success of e-commerce. In our research paper we present a standard model to analytically identify and position the confidence relationships that need to be established in any e-commerce activity. Considering the fact that information security is the major contributor of the general confidence for e-commerce, the paper also illustrates the role of information security as an integral part of the overall confidence in electronic transactions.

Keywords *—threat, security, payment system, e-commerce, authentication*

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I. INTRODUCTION

Requirement of confidence is significant problem on the way of e-commerce success [1]. The parties involved in any commerce must feel confidence in the people and companies with whom they do commerce. In many traditional commerce relationships, confidence is based on a combination of judgment or opinion based on face-to-face meetings, or recommendations of colleagues, friends and commerce partners. However, Internet based commerce generally does not involve human interaction and, therefore, this new context requires a new understanding of confidence. Confidence must be established and managed continuously in a wide range of e-commerce activities such as a group of transactions, a given transaction, a transaction phase, and an action within a commerce phase. The first step towards establishing confidence is to be able to depend on the computing and communication system. Dependability can be seen as a system property consisting of security, reliability, availability, safety, timeliness, and maintainability attributes [3], [2]. [3] Also identifies the following requirements for establishing confidence: trusting commerce partners and their systems, the ability of tracing and identifying products, managing risks on an ongoing basis, existence of a legal framework to fall back on, transparency ease of system use, and privacy. Confidence management, being out of our scope here, exploits the properties of confidence such as: confidence is relative, directed, measurable, existing in time, evolving, and transferable [2].

II. TRANSACTIONS AND CONFIDENCE

Every commerce transaction can be viewed as a finite set of actions between commerce actors. The goal is to initiate, arrange and complete a contractual agreement for exchange of goods, services, information or funds. In each commerce transaction some artifacts are exchanged. An artifact is referred to any logical or physical passive object such as products, messages, contracts, etc. Most artifacts in e-commerce are digital documents that have to be confidence relation there exist a relying party and a trusted party. When such a relation is established, we say that the former one confidences the latter one. In practice, the confidence relationship between two parties is mutual, normally of different type or degree in either direction. We will not elaborate on such mutuality because it can be seen as two (non-identical) confidence relationships in opposite directions. Let's assume two parties are directly involved in an action whereby a digital artifact is transferred. We examine the confidence relationship from the receiver (the relying party) to the sender (the trusted party) of the artifact. The established confidence relation is the outcome of three confidence binds located at the commerce, personal and physical layers (see the figure).

- T1) Commerce layer confidence, where the organizations rely on their peers.
- T2) Personal layer confidence, where people /agents behind the flow of the physical goods confidence each other.
- T3) Physical layer confidence, where the transfer process of physical objects is trusted.

The depth and nature of the layers mentioned above depend on the type and role of the actors involved, as well as on the context of the corresponding commerce activity. Having all these horizontal confidence T1, T2 and T3 is necessary (and sufficient) to establish the confidence relationship from the relying party to the trusted party. The established physical confidence (and therefore the artifact) plays an important role in inducing confidence at the personal and commerce layers. To this end, it is necessary to tightly couple the layers of the model by setting up vertical confidence relations between layers. Consider again the process of transferring digital data from the trusted party to the relying party. The necessary confidence relations are:

- T4) Human resources: The relying party's organization confidence its employee to operate honestly.
- T5) Dependability: The relying party's employee confidences his terminal to function appropriately.
- T6) Authenticity: The trusted party's PC has to be sure about the identity of the person sending the data.
- T7) Accountability: The trusted party's employee must be assured of her/his organization's support to carry out the transfer.

Note that, besides T3, confidences T5 and T6 are necessary (perhaps not sufficient) to establish the personal-to-personal confidence relationship T2. Similarly, vertical confidences T4 and T7 play their roles in establishing the commerce-to-commerce confidence T1. The "not sufficient condition" is because what perceived from previous experiences, for example, also plays a role in inducing T1 and T2. The overall confidence in an e-commerce transaction requires a coupling force to bind all activities in the commerce transaction. For example, in a typical commerce transaction, the activity of obtaining a letter of credit is an essential step towards such binding confidence. This establishes confidence at a higher level abstraction. The concept of the layered model can also be used to model such a transaction confidence.

III. SECURITY AND CONFIDENCE

Information security threats include communication and resource related threats. Security services offering protection from security threats are: identification, authentication, confidentiality, integrity, access control, and non-reputation. Information security is an integral part of confidence. The scope of issues mentioned above. This section tries to clarify the position of (information) security in providing confidence within a commerce activity where a digital item is transferred. Information security measures reside in the physical layer of the confidence model and have interactions with the personal layer via T5 and T6. The table below illustrates the relation between the main confidence requirements of e-commerce, mentioned in Section 1, and the components of the confidence model. Symbol "Y" in a row indicates that the corresponding confidence component is also needed to establish the confidence component marked by "X" in that row. Furthermore, symbol "(Y)" indicates that the corresponding confidence component might be examined in providing the security service in that row. Of special interest in this table is the domain of requirements that information security services (pertaining to the corresponding requirements) cover, see the marked square in the table.

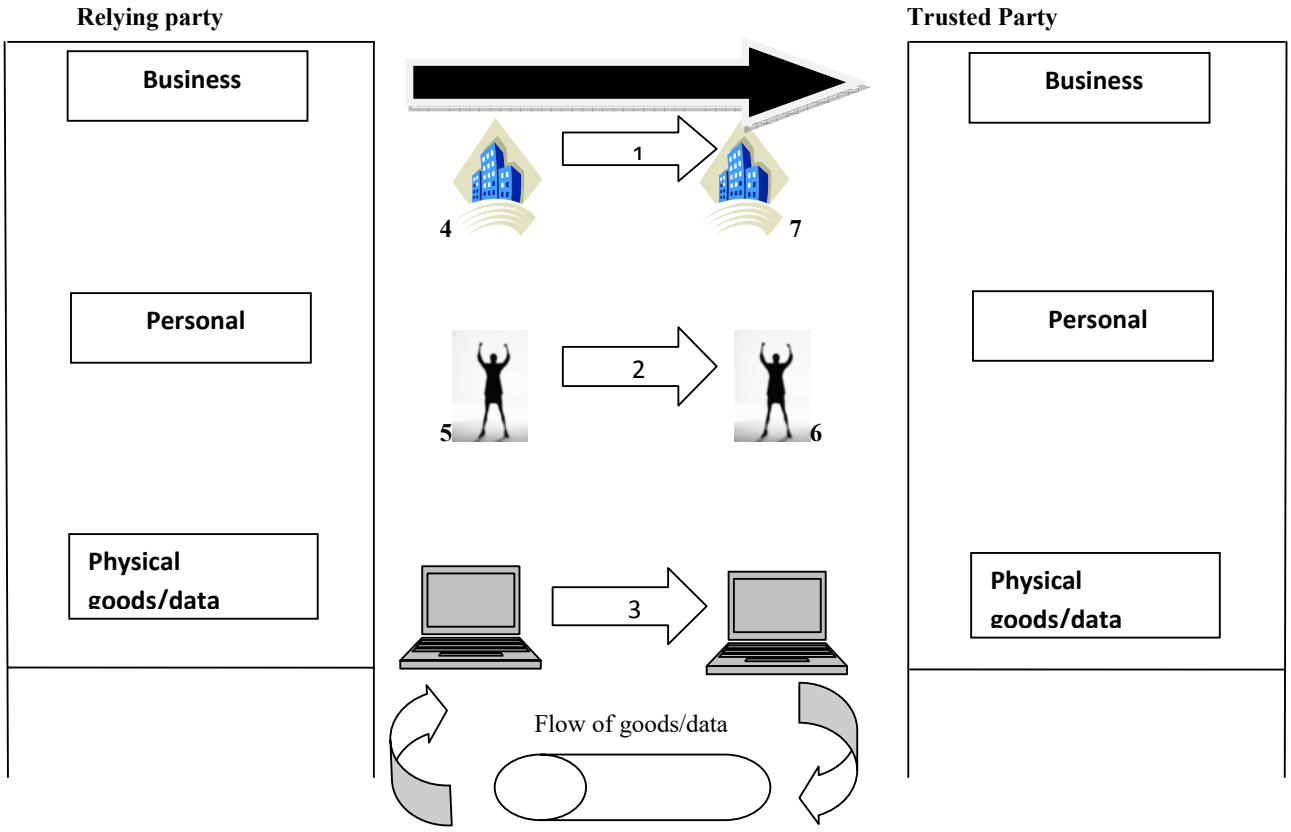

Figure 1. A model of confidence for E-commerce

Table 1 REQUIREMENTS OF CONFIDENCE

Trust requirement	Trust components in the model						
	T1	T2	T3	T4	T5	T6	T7
Reliability of e-business partners	X						
Identity of e-business partners	X			Y	Y	Y	Y
Risk management (on information)	X	X					

IV. CONCLUSION

Confidence in the context of e-commerce is for a large part covered by dependability. Missing, however, are commerce and personal requirements as well as bindings between commerce and personal levels? Means to cover these are available, but not fully understood. Trusted third parties can help confidence commerce's. Personal training, human resource developments and good organizational procedures can help accountability and human resource factors.

A balanced view of all these elements in relation to security factors is still missing. This is the subject of a larger study within confidence establishment; evaluation and management are set to be studied in the scope of our long term research. Particularly, our goal is to formalize a method for designing confidence full e-commerce applications. In this paper we took the first step to position the confidence bindings necessary in e-commerce transactions and illustrated the role of security services in this regard.

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TELEMATICS AND INFOTAINMENT SYSTEM IN VEHICLES BASED ON ANDROID (TISIVA!)

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Abstract— android is an open source operating system for mobile devices and small term computers which is based on the Linux Kernel and the software stack runs on a Java based object oriented framework. We propose an idea to build an Android in-vehicle system to help the user drive more safely as well as efficiently. The system named TISIVA will run with the help of an x86 system running the Android OS and its subsequent API (application programming interface). This system uses inputs from various hardware devices like Accelerometer, Proximity Sensors, Vehicle ODB Interface, and Environment Sensors in combination with services like GPS and Internet to improve safety of driving and also provide infotainment services for the passengers. Based on our study, we will be able to build a minimal functionality system at a very affordable cost of about twenty to thirty thousand rupees. Our system is open source unlike existing proprietary systems and will also support applications downloaded from Android Market and also other third party developed applications.

Keywords - *Android, Car management, Google Maps API*

I. INTRODUCTION

Since android is an open source operating system it is easy to develop applications using java and as well as the native language and then converting it into the Android Classes. The idea what is been proposed is to have a basic 1 GHz computer system running in the car with Android operating system being the sole controller. The system is eing interfaced with the vehicle ECU and the sensors and it helps the user to have a better control over the vehicle. The reason why we chose Android 3.2 over other operating systems is that it enables android powered devices to act as USB hosts. That means we can use them with a whole host of peripheral devices and development boards that have USB connectivity. And Android 3.2 comes with another feature that allows the android OS to run on devices other than a mobile phone or a tablet. So it can be run on devices like laptops and PCs. And programming and main OS features will be exactly same as that of the previous android versions. And programmers will be abstracted from the variations in hardware and will only need to concentrate on developing their app rather than worrying about the Hardware on which they would be implemented so based on all these; we propose an Android based in-vehicle Telematics and Infotainment System. Android will be running in the core of the system and various applications developed by the manufacturer of the vehicle and third party applications will run over it and they will utilize data from GPS, Accelerometer, Proximity sensor, and RAW data coming from the Vehicle's internal systems to provide a better and safer driving experience for the drivers and the passengers. Since our system runs on android and has several networking capabilities, it can easily pair with an Android Smart Phone or a tablet. This allows interoperability between TISIVA and the handheld device. This means TISIVA can be controlled using our handheld and at the same time, the TISIVA can integrate and manage the handheld device. This allows calls and other communications to be routed to TISIVA which allows drivers to easily communicate without having to use their handheld phones. The TISIVA can be controlled using any Android based handheld device. The Android device can be connected to TISIVA using WLAN (IEEE 802.11) or through IP. Few of the features that our System supports is

- Drunken Drive Detection
- Automatic Over speed Detection
- Car Tracking
- Voice Applications using Google
- Voice SMS
- Unlimited Entertainment Features
- Car Maintenance reminder
- Engine performance Reports

These are only few of the applications; the features in our system can be expanded based on the user requirements. The other features are well briefed in the paper.

II. WHY ANDROID?

The advantage of using Android is that every vehicle irrespective of the manufacturer will have a common software interface (Android). And android is open source and free and already available, so there is no need to put in a lot of money on development of a

new Car OS system. And also that Android has moved more from an OS to being a trend today. The amount of apps (applications) provided in the Android market is so plenty that it beats the iOS to be the best mobile OS today

III. EXISTING SYSTEM IN CARS

The existing system in cars for the speedometers, tachometer, the fuel consumption and all the features are pretty analog unless the user is ready to go for a high rated car over 25lakhs. When focusing on mid-range cars which cover 90% of the population in India the user is only given features worth his money which is all analog and manual. For example, the mileage of a car can be only calculated manually in a mid-range car. These systems tend to be maintained frequently and they cannot be developed further to meet the user's requirements. It is also costly to reinstall this system.

A. Disadvantages of the Existing System

There are various disadvantages that one faces in the existing system and these are the few reasons we feel our system is better off at

- Analog Statistics
- Not accurate values
- Manual Security may tend to be dangerous
- Complication in Electrics and Electronics
- The features cannot be expanded since it is not digital.
- Systems cannot be extended because of proprietary software and hardware
- Maintenance cost

These are the disadvantages that one faces using the existing system of cars. Unless a person can afford a high valued car with top notch features he won't be able to attain accuracy and safety for his vehicle. This glitch can be overcome by our system

IV. ORE SYSTEM MODEL DESIGN

Instead of spending much on a high end car our system is well suited to the mid-range cars. A user who is ready to invest around 5-6 lakhs on a car can as well spend another twenty or thirty thousand on TISIVA which makes his car equivalent to the high end car. There are number of key requisites that our system requires which does not cost more than a few thousands.

A. CPU

- Optimized system for running Linux-based
- Operating systems
- Low power consumption of just 8W-11W per board (in use)
- 1.6GHz processor (Intel Atom Z530 CPU)
- 2GB RAM
- 2.5" IDE and SATA connectors, for a 2.5” hard drive or sold state drive (SSD)
- Compact Flash card slot
- 2 x USB 2.0 ports
- 2 x mini PCI sockets
- 1 x serial port (RS232)
- 1 x GigE Ethernet port, 2 x 10/100 Ethernet ports
- All the lowest requirements needed to build our system.

B. Interface Board-Arduino Development Board:

Arduino is an open-source electronics prototyping platform based on flexible, easy-to-use hardware and software. It's intended for artists, designers, hobbyists, and anyone interested in creating interactive objects or environments. Arduino Development Boards interfaces to above IO systems through "Shields" and Arduino board connect to the core CPU through Android's USB Accessory Interface.

C. Input Devices Supported:

Few input devices supported by the system are

ADC / DAC

- ArduStat- (Measures charge in battery)
- Audio
- Capacitive Sensing
- Distance Sensing
- Environmental Sensing
- Humidity
- Temperature

- Images
- Joysticks / Gamepads
- Keyboard/Keypads
- Location- GPS, etc.
- Magnetic
- Magnetic Cards
- Mice
- Motion Sensors
- Position Sensing
- Pressure Sensors
- RFID tag reading
- Slotted Detectors / Proximity Sensors
- Touch screen

All Sensors can be managed by a General Purpose Sensor abstraction layer (One interface to setup and control most Digital and analog sensors)

D. Output:

In the visual end the output can be via various displays that include

- LED Lights and Displays
- LCDs
- Video
- Physical/Mechanical
- Electrical / High Power
- Multiplexing outputs
- USB

In the audio section there are

- Real-time audio processing
- Tone Generation Libraries
- Synthesizers and sound generation
- Speech synthesis / Voice synthesis
- MIDI

E. Communication options

The various communication options provided by our system are

- Ethernet
- Serial
- GSM/GPRS
- Wi-Fi

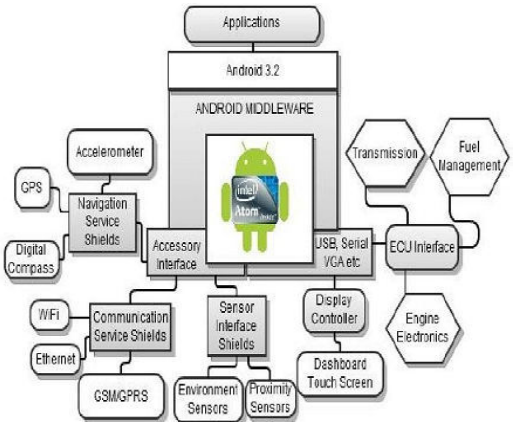

Fig 1 the block diagram explaining the interfacing of our Android system onto the vehicle and its usage.

V. SOFTWARE APPLICATIONS

The system that we proposed has number of applications which help the user to make better use of the car in ways of security, entertainment, information as well as creativity in developing customized apps for his system.

A. Voice Control

This is one of the main features of our system. We aim to provide safety for the driver and also ease of access to various features of our system. Natural Language processing has improved so much that recognizing human speech is not a difficult task anymore. In our system we also implement a voice recognition system using the Google Speech Engine API that will allow users of the system to interact with the system or with the car rather, using voice commands. For instance, the windshield wipers, indicators, Air Condition Systems etc. can be controlled using voice commands. Also our system adds safety to the car, since, this system when integrated with an Android handheld device helps the user to send text messages using their voice. The user can just talk into their hands free which is recognized by Google recognition and converted to text which is sent as a message and when the user receives a text it

is again converted to voice and fed to the hands free. Thus this helps the user to give him concentration on the road rather his mobile device. The growth of messaging is so vast today that it is also the reason for the recent growth of accidents on the road today. Our system gives an alternative to those users whose messaging is one of their key works.

B. Car Tracking Applications

Nowadays, shopping malls, cinema theatres are becoming bigger and large crowds visit them each day and almost all of them come in cars. Once the car is parked in the malls it is difficult to identify them once we are back. We can locate car using our handheld device which has been paired with TISIVA. The software running on the handheld will send a notification signal to TISIVA to which the TISIVA will respond with the GPS coordinates of the car received using the onboard GPS receiver. This allows us to easily locate our car. This can be useful when your car gets stolen also.

C.ODB Integration

The OBD (On-Board Diagnostics) port under the dash is where a mechanic normally plugs in a laptop to run diagnostics on the engine management system. The Android application in TISIVA that is monitoring the Interface is permanently connected to the port and polls the ECU every few seconds to store dozens of parameters about vehicle performance including speed, RPM, intake manifold air temperature, engine load, fuel level, fuel pressure, fuel injection mode, timing, and many other items. All data is stored indefinitely in a SQLite database. The error codes that the ODB provides tell the user what exactly has gone wrong in the car. Generally only mechanics can understand and diagnose the error codes provided by the ODB. But TISIVA will maintain a database of all such error codes for the particular car and will provide information directly to the driver and hence the driver will have good knowledge of what exactly is going on in his car. Moreover if TISIVA is connected to the internet, it will search for more information about the problem and may be possible solutions also. The features include

- Acceleration (0 - 60, 0 - 100, X - Y, etc.)
- Deceleration (0 - 60 - 0, 0 - 100 - 0, etc.)
- Elapsed Time (1/4mi, 1/8mi, etc.)
- Custom Tests.
- Top Speed.

D. Remote Controlling of TISIVA

As mentioned earlier, the TISIVA can be controlled using any Android based handheld device. The Android device can be connected to TISIVA using WLAN (IEEE 802.11) or through IP if the car owner has installed an Internet Connectivity device (say, A Wireless Modem) in the car's system. Thus this will allow the car owner to perform a lot of tasks like unlocking the car, opening boot, opening the bonnet, sounding the horn, turning on the AC etc. using the handheld device. We will provide an application for the phone which will provide a user-friendly interface to TISIVA.

E. Integrated Location Information

A standard GPS receiver just provides a map and pinpoints your location on the map and also may show the path to your destination. But our system is beyond that. Since we integrate Google maps in our system, we will be able to access a lot of human created content that is generally available on Google maps like info about restaurants, cheap hotels, places of interest etc. We will also integrate Social Networking into our system by using the API provided by Facebook, Twitter etc. to extract information about the places you might be interested within few miles of your current location. It can also provide the elapsed time to reach a destination. Using Google Maps we can also send alerts when the user is passing the school zone or hospital zones and other no horn zones.

F. Security systems

The Android Security Car System will be able to recognize objects around the road/highway and take decisions to prevent crash accidents. The system has many camera extensions and is able to recognize what object is near/far, it can calculate the speed who the object has and if the object is dangerous or has an imminent crashing state the car can take decisions like stop, activate air bags security system, etc., before the impact. For that the system will be able to recognize images trough the cameras and to know if the object is a human, a car or other stuff, all of this to know if it can active or not the security system. The system has applications to know the state of the road to take decisions to keep the stability of the car, thanks to the sensibility of the accelerometer. In case of crash accident the system should take decisions and keep the stability of the car. The system will keep in memory (black box, hard drive, etc.) all the information log after a crash accident to help to understand what was the cause.

VI. FUTURE WORKS

Along with this idea proposed by us we are trying to implement this model on a small term basis and try to

experiment with other hybrids in the world of ndroid development. We would come out with the implementation of the above idea proposed if essentials pertained.

VII. CONCLUSIONS

The above idea proposed is an economic alternative to the high budgeted cars in today's market. If given a proper backbone to this project it would create a revolution equivalent to the buzz what Android has created in the mobile phone sector. This idea is cost efficient and is more controlled by the user than the manufacturer which would be the one of the main reason this system would sell.

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ELECTRONIC PESTICIDE USING SOLAR ENERGY WITH MOBILE CONTROL ROBOT

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Abstract— Pesticides are most essential factor in the agricultural sector. Chemical pesticides kill the pests & protect the crops. It is necessary to protect the crops for high yield. But chemical pesticides not only bring the problem of health hazards but also problem of pollution such as air, soil & water. Therefore this has been serious issue now days. To solve all these problems we have constructed Electronic Pesticide. In this paper, working principle of Electronic pesticide, its construction details & its effects are discussed.

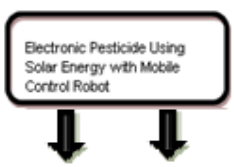
Keywords— *Electronic pesticide, inverter, voltage multiplier, D.T.M.F. Robot, Solar energy*

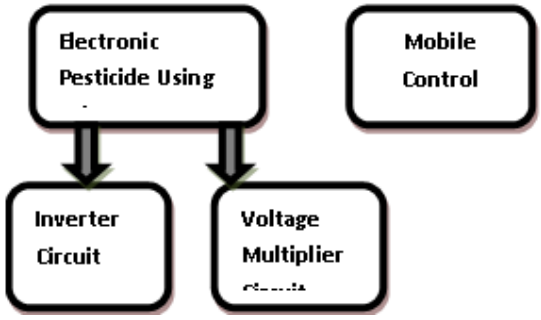
I. INTRODUCTION

Pesticides are most essential factor in the agricultural sector. Chemical pesticides kill the pests & protect the crops. It is necessary to protect the crops for high yield. But chemical pesticides not only bring the problem of health hazards but also problem of pollution such as air, soil & water. Therefore this has been serious issue now days. In agriculture, mostly chemical pesticides are used to control pests. But chemical pesticides have many harmful effects on human body as well as environment. Again some pests develops resistivity again pesticides & it is difficult to control such pests using pesticides.Therefore Electronic pesticide is the best replacement of chemical pesticides. Electronic pesticide kill pest more effectively than chemical pesticides as well as it is more cost effective than chemical pesticide with less harmful effect on human health as well as environment.

Electronic pesticide works on high voltage. The electronic pesticide is nothing but combination of inverter & voltage multiplier. Inverter converts DC supply to AC supply & voltage multiplier multiply that voltage, high enough to at least break down the dielectric formed when an insect comes close enough to the mesh. An electrical arc is formed when the dielectric breaks down & current flows through the insect's body. The insect is electrocuted & then dried & killed. Solar cell is used as input for inverter. Electronic pesticide Circuit with CFL bulb (to attract the insects) is mounted on Mobile Control Robot. With the help of Mobile Control Robot, we can move electronic pesticide in all fields from remote location also.

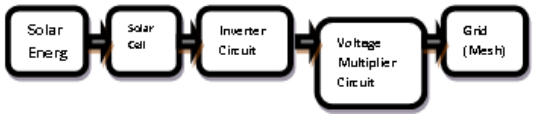
II. TECHNICAL ASPECT OF PROPOSED SOLUTION



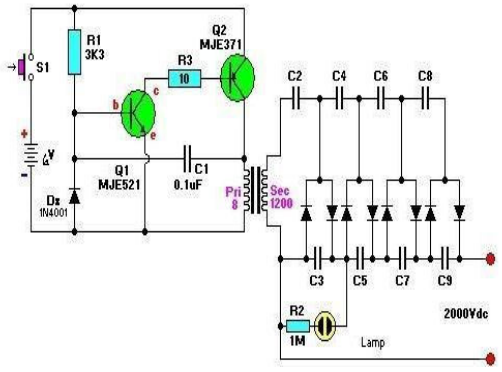


This project i.e. Electronic Pesticide using solar energy with mobile control robot is divided into two parts (1) Electronic pesticide using solar energy (2) Mobile control robot. Further Electronic pesticide using solar energy is subdivided into (a) Inverter circuit & (b) Voltage multiplier circuit.

ELECTRONIC PECTICIDES USING SOLAR ENERGY BLOCK DIAGRAM



INVERTER & VOLTAGE MULTIPLIER CIRCUIT

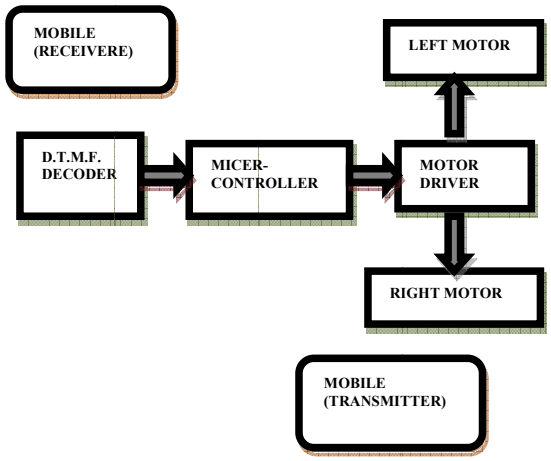


PARTS LIST OF INVERTER & VOLTAGE MULTIPIER CIRCUIT

Q1	MJE521
Q2	MJE371
C1,C2,C3,C4,C5,C6,C7,C8,C9	0.1 uF
Transformer	Step-up
D	1N4001
R1	3K
R2	1M
R3	10
Battery	6V
Switch	S1

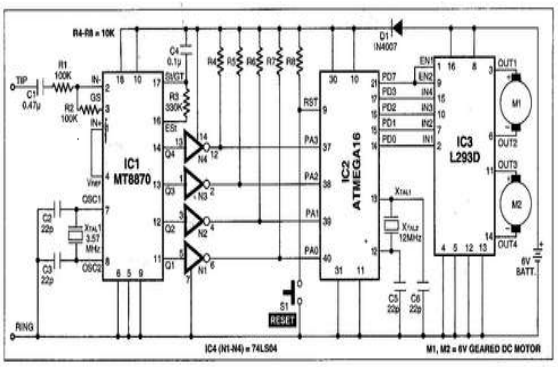
WORKING OF ELECTRONIC PESTICIDES

Electronic pesticide is a device that attracts and kills insects that are attracted by light. A light source attracts insects to an electrical grid, where they are electrocuted by touching two wires with a high voltage between them. A light source is fitted inside, wire meshes designed to emit ultraviolet light, which is visible to and attracts insects. The light is surrounded by a pair of interleaved wire grids or spirals. The distance between adjacent wires is typically about 2 mm. A high-voltage power supply powered by solar cell which may be a simple voltage multiplier circuit made with diodes and capacitors, generates a voltage of 2,000 volts or more, high enough to conduct through the body of an insect which bridges the two grids, but not high enough to spark across the air gap. Enough electrical current flows through the small body of the insect to heat it to a high temperature. The impedance of the power supply and the arrangement of the grid is such that it cannot drive a dangerous current through the body of a larger animal (human, bull,etc).The Inverter takes 6 volt d.c and steps it up to 120 volt a.c. The wattage depends on which transistors used for Q1 and Q2, as well as the "Amp Rating" of the transformer you use for T1. Voltage multiplier circuit is powered by 220v AC. This circuit produces a high voltage but very minimal current.



Mobile Control Robot Block Diagram

CIRCUIT OF MOBILE CONTROL ROBOT



PARTS LIST OF MOBILE CONTROL ROBOT

DECODER	MT8870 DTMF
MICRO-CONTROLLER	ATmega16 AVR
MOTOR DRIVER	L293D
NOT GARE	74LS04
RECTIFIER DIODE	1N4007
RESISTANCE (R1,R2)	100-kilo-ohm
RESISTANCE (R3)	330-kilo-ohm
RESISTANCE (R4-R8)	10-kilo-ohm
CAPACITORS (C1)	0.47µF ceramic disk
CAPACITORS (C2,C3,C5,C6)	22pF ceramic disk
CAPACITORS (C4)	0.1µF ceramic disk
XTAL1 crystal	3.57MHz
XTAL2 crystal	12MHz
Push-to-on switch	S1
DC MOTOR (M1,M2)	12V, 50-rpm geared
BATTERY	12V, 4.5Ah

CIRCUIT DISCRIPTION OF MOBILE CONTROL ROBOT

In this project, the robot is controlled by a mobile phone that makes a call to the mobile phone attached to the robot. In the course of a call, if any button is pressed a tone corresponding to the button pressed is heard at the other end of the call. This tone is called 'dual-tone multiple-frequency' (DTMF) tone. The robot perceives this DTMF tone with the help of the phone stacked in the robot. The received tone is processed by the ATmega16 microcontroller with the help of DTMF decoder MT8870. The decoder decodes the DTMF tone into its equivalent binary digit and this binary number is sent to the microcontroller. The microcontroller is pre programmed to take a decision for any given input and outputs its decision to motor drivers in order to drive the motors for forward or backward motion or a turn. The mobile that makes a call to the mobile phone stacked in the robot acts as a remote. So this simple robotic project does not require the construction of receiver and transmitter units. DTMF signaling is used for telephone signaling over the line in the voice-frequency band to the call switching

centre. The version of DTMF used for telephone tone dialing is known as 'Touch-Tone.' DTMF assigns a specific frequency (consisting of two separate tones) to each key so that it can easily be identified by the electronic circuit. The signal generated by the DTMF encoder is a direct algebraic summation, in real time, of the amplitudes of two sine (cosine) waves of different frequencies, i.e., pressing '5' will send a tone made by adding 1336 Hz and 770 Hz to the other end of the line. The tones and assignments in a DTMF system are shown in Table

TONES & ASSIGNMENTS IN ASSIGNMENT IN D.T.M.F. SYSTEM

Frequencies	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

D.T.M.F. DATA O/P

Low Group (Hz)	High Group (Hz)	Digit	OE	D3	D2	D1	D0
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	H	H	L	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
---	---	ANY	L	Z	Z	Z	Z

ACTION PERFORMED CORRESPONDING TO THE KEY PRESSED

Number Pressed By Users	O/P of HT9170 DTMF Decoder	I/P to Micro-controller	O/P from Micro-controller	Action Performed
2	0x02 00000010	0XFD 11111101	0x89 10001001	Forward Motion
4	0x04 0000010	0XFB 1111101	0x85 1000010	Left Turn
	0	1	1	
6	0x06 00000110	0XF9 11111001	0x8A 10001010	Right Turn
8	0x08 00001000	0XF7 11110111	0x86 10000110	Backward Motion
5	0x05 00000101	0XFA 11111010	0x00 00000000	Stop

The block diagram of the microcontroller-based mobile phone operated land rover. The important components of this rover are a DTMF decoder, microcontroller and motor driver. An MT8870 series DTMF decoder is used here. All types of the MT8870 series use digital counting techniques to detect and decode all the 16 DTMF tone pairs into a 4-bit code output. The built-in dial tone rejection circuit eliminates the need for pre-filtering. When the input signal given at pin 2 (IN-) in single-ended input configuration is recognized to be effective, the correct 4-bit decode signal of the DTMF tone is transferred to Q1 (pin 11) through Q4 (pin 14) outputs. Table shows the DTMF data output table of MT8870. Q1 through Q4 outputs of the DTMF decoder (IC1) are connected to port pins PA0 through PA3 of ATmega16 microcontroller (IC2) after inversion by N1 through N4, respectively. The ATmega16 is a low-power, 8-bit, CMOS microcontroller based on the AVR enhanced RISC architecture. It provides the following features: 16 kB of in-system programmable Flash program memory with read-while-write capabilities, 512 bytes of EEPROM, 1kB SRAM, 32 general-purpose input/output (I/O) lines and 32 general-purpose working registers. All the 32 registers are directly connected to the arithmetic logic unit, allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code-efficient. Outputs from port pins PD0 through PD3 and PD7 of the microcontroller are fed to inputs IN1 through IN4 and enable pins (EN1 and EN2) of motor driver L293D, respectively, to drive two geared DC motors. Switch S1 is used for manual reset. The microcontroller output is not sufficient to drive the DC motors, so current drivers are required for motor rotation. The L293D is a quad, high-current, half-H driver designed to provide bidirectional drive currents of up to 600 mA at voltages from 4.5V to 36V. It makes it easier to drive the DC motors. The L293D consists of four drivers. Pins IN1 through IN4 and OUT1 through OUT4 are input and output pins, respectively, of driver 1 through driver 4. Drivers 1 and 2, and drivers 3 and 4 are enabled by enable pin 1 (EN1) and pin 9 (EN2), respectively. When enable input EN1 (pin1) is high, drivers 1 and 2 are enabled and the outputs corresponding to their inputs are active. Similarly, enable input EN2 (pin 9) enables drivers 3 and 4.

SOFTWEAR DESCRIPTION

The software is written in 'C' language and compiled using Code Vision AVR 'C' compiler. The source program is converted into hex code by the compiler.Burn this hex code into ATmega16 AVR microcontroller. The source program is well commented and easy to understand. First include the register name defined specifically for ATmega16 and also declare the variable. Set port A as the input and port D as the output. The program will run forever by using 'while' loop. Under 'while' loop, read port A and test the received input using 'switch'Statement. The corresponding data will output at port D after testing of the Received data. To charge the battery we can use solar energy.

Source program:
Robit.c

```
#include <mega16.h>
void main(void)
{
unsigned int k, h;
DDRA=0x00;
DDRD=0XFF;
while (1)
{
k =~PINA;
h=k & 0x0F;
switch (h)
{
case 0x02: //if I/P is 0x02
{
PORTD=0x89;//O/P 0x89 ie Forward
break;
}
case 0x08: //if I/P is 0x08
{
PORTD=0x86; //O/P 0x86 ie Backward
break;
}
case 0x04:
{
PORTD=0x85; // Left turn
break;
}
case 0x06:
{
PORTD=0x8A; // Right turn
break;
}
case 0x05:
{
PORTD=0x00; // Stop
break;
}
}
}
}
```

WORKING

In order to control the robot, you need to make a call to the cell phone Attached to the robot (through head phone) from any phone, which sends? DTMF tunes on pressing the numeric buttons. The cell phone in the robot is kept in 'auto answer' mode. (If the mobile does not have the auto answering facility, receive the call by 'OK' key on the rover-connected mobile and then made it in hands-free mode.) So after a ring, the cell phone accepts the call. Now you may press any button on your mobile to perform actions as listed in Table III. The DTMF tones thus produced are received by the cell phone in the robot. These tones are fed to the circuit by the headset of the cell phone. The MT8870 decodes the received tone and sends the equivalent binary number to the microcontroller. According to the program in the microcontroller, the robot starts moving. When you press key '2' (binary equivalent 00000010) on your mobile phone, the microcontroller outputs '10001001' binary equivalent. Port pins PD0, PD3 and PD7 are high. The high output at PD7 of the microcontroller drives the motor driver (L293D). Port pins PD0 and PD3 drive motors M1 and M2 in forward direction (as per Table III).Similarly, motors M1 and M2 move for left turn, right turn, backward motion and stop condition as per table.

CONSTRUCTION OF MOBILE CONTRO ROBOT

When constructing any robot, one major mechanical constraint is the number of motors being used. You can have either a two-wheel drive or a four-wheel drive. Though four-wheel drive is more complex than two-wheel drive, it provides more torque and good control. Two-wheel drive, on the other hand, is very easy to construct. Top view of a four-wheel-drive land rover is shown in Fig. 3. The chassis used in this model is a 10×18cm2 sheet made up of parax.Motors are fixed to the bottom of this sheet and the circuit is affixed firmly on top of the sheet. A cell phone is also mounted on the sheet as shown in the picture. In the four-wheel drive system, the two motors on a side are controlled in parallel. So a single L293D driver IC can drive the rover. For this robot, beads affixed with glue act as support wheels.

PERFORMANCE ESTIMATION OF THE SOLUTION

Sr. No.	Part Of Project	Cost
(1)	Electronic Pesticide (Inverter Circuit + Voltage Multiplier Circuit)	Rs 1000
(2)	Mobile Control Robot (without cost of mobile)	Rs 1000
(3)	Solar Cell	Rs 1500
	Total	Rs 3500

PROS & CONS OF SOLUTION
Advantages:-

(1) Harmful effect on human health due to chemical pesticides, completely avoided by electronic pesticide.
(2) Electronic pesticide also helps in reducing pollutions like air, water & soil.
(3) Solar energy is used to give input to the inverter. So energy conservation is there.
(4) Mobile control robot is mounted on mobile control robot; it helps to control motion of Electronic pesticide from remote area.
(5) Single Electronic pesticide Circuit is used in whole field along with mobile control robot, it reduces the cost .So it also helps in money saving.
(6) Electronic pesticide kills the pest effectively than chemical pesticide .It also kills non-flying pest by attracting them using hormones, but it requires manual operation.
(7) It also helps to control MALERIA in villages as it works better than DDT powder.

Disadvantages:-

(1) Electronic pesticide kills useful insects also.
(2) CFL is used to attract the pests. Therefore this pest control method used only night hours only.
(3) During rainy season due to mud it is difficult to use mobile control robot.Hense it is better to mount Electronic pesticide on a pole in the field. As a result of this sufficient no. of poles are required to control pest in the whole field .So it is somewhat costlier than mobile control robot, but cheaper than chemical pesticide .

RESULT

Electronic pesticides kill almost all flying pest as result of it we can break life cycle of pests & we can control 60% pest in next generation. Simultaneously we can reduce harmful effect of chemical pesticides on human health as well as environment (water, air& soil pollution).

CONCLUSION

Electronic pesticide is the best replacement of chemical pesticides. Electronic pesticide kill pest more effectively than chemical pesticides as well as it is more cost effective than chemical pesticide with less harmful effect on human health as well as environment.

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CLOUD COMPUTING AN AMICABLE STORAGE ABYSS ON THE CLOUD SERVICING THE HEALTH SECTOR.

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Abstract:- The advent of cloud computing- a pervasive force which is working its way into all aspects of civilization has in turn paved way for several network based malware and attacks to proliferate rapidly through it. The fact that the cloud was not developed with principles of security in mind calls for several security measures to be adopted and implemented. Though several such cloud based security mechanisms are being proposed and put to work in large numbers, they work in an incoherent fashion making the cloud vulnerable to attacks. Insecurity is growing at an exponential rate proportional to the immense growth of cloud service providers. This paper suggests a way to mitigate indulgence in user privacy on a cloud based environment by deploying a third party server on the cloud that would assure users some solid privacy and security by means of which securing the users data on the cloud will become a bright possibility rather than a mere probability. We have proposed a way by which data exchange and collection in the different sectors would be amicable. Thus trowing light into the areas of high scale data exchange, we would say "Security threats ail data exchange while our cloud aids it"

I. INTRODUCTION.

Today there is an immense growth in the companies that are established online. Companies like Flipkart , OLX have established their own server and retail chain, to provide service to the customers. Not many know how these companies actually function and manage a profit. The answer is cloud ! Cloud, is nothing but the internet. AAA – Anything Anywhere Anytime is the idea behind cloud computing. These Companies can greatly reduce IT costs by offloading data and computation to cloud computing services. Still, many companies are reluctant to do so, mostly due to outstanding security concerns. A recent study surveyed more than 500 chief executives and IT managers in 17 countries, and found that despite the potential benefits, executives trust existing internal systems over cloud-based systems due to fear about security threats and loss of control of data and systems.

II. EXISTING SCENARIO

One of the most serious concerns today in cloud based services is the possibility of confidentiality violations. Either maliciously or accidentally, cloud provider's employees can tamper with or leak a company's data. Such actions can severely damage the reputation or finances of a company. In order to prevent confidentiality violations, cloud services' customers might resort to encryption. While encryption is effective in securing data before it is stored at the provider, it cannot be applied in services where data is to be computed, since the unencrypted data must reside in the memory of the host running the computation. In Infrastructure as a Service (IaaS) cloud services such as Amazon's EC2, dropbox , the provider hosts virtual machines (VMs) on behalf of its customers, who can do arbitrary computations. In these systems, anyone with privileged access to the host can read or manipulate a customer's data. Consequently, customers cannot protect their VMs on their own. Cloud service providers are making a substantial effort to secure their systems, in order to minimize the threat of insider attacks, and reinforce the confidence of customers. For example, they protect and restrict access to the hardware facilities, adopt stringent accountability and auditing procedures, and minimize the number of staff who have access to critical components of the infrastructure. Nevertheless, insiders who administer the software systems at the provider back end ultimately still possess the technical means to access customers' VMs.

Thus, there is a clear need for a technical solution that guarantees the confidentiality and integrity of computation in a way, that is verifiable by the customers opting for the cloud based services.

III. BACKGROUND

A. Infrastructure as a Service : An insight into the existing storage services on the cloud. Today, myriads of cloud providers offer services at various layers of the software stack. At lower layers, Infrastructure as a Service (IaaS) providers such as Amazon, Flexiscale, Dropbox and GoGrid allow their customers to have access to entire **V**irtual **M**achines (VMs) hosted by the provider. A customer, and user of the system, is responsible for providing the entire software stack running inside a VM. At higher layers, Software as a Service (SaaS) systems such as Google Apps offer complete online applications than can be directly executed by their users.The difficulty in guaranteeing the confidentiality of computations increases for services sitting on higher layers of the software stack, because services themselves provide and run the software that directly manipulates

customer's data (e.g., Google Docs). In this paper we focus on the lower layer IaaS cloud providers where securing a customer's VM is more manageable and amicable.

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B. The Attack model

A system administrator of the cloud provider who has privileged control over the back end can perpetrate many attacks in order to access the memory of a customer's Virtual Machine. With root privileges at each machine, the system administrator can install or execute all sorts of software to perform an attack. The system administrator directly accesses the content of a VM's memory at run time. Furthermore, with physical access to the machine, a system administrator can perform more sophisticated attacks like cold boot attacks and even tamper with the hardware. In current IaaS providers, we can reasonably consider that no single person accumulates all these privileges. Moreover, providers already deploy stringent security devices, restricted access control policies, and surveillance mechanisms to protect the physical integrity of the hardware.
Nevertheless, system administrators need privileged permissions at the cluster's machines in order to manage the software they run. Since we do not precisely know the praxis of current IaaS providers, we assume in our attack model that system administrator can login remotely to any machine with root privileges, at any point of time. The only way a system administrator would be able to gain physical access to a node running a costumer's VM is by diverting this VM to a machine under his/her control, located outside the IaaS's security perimeter. Therefore, a protocol deployed must be able to

1. confine the VM execution inside the perimeter, and
2. guarantee that at any point a system administrator with root privileges remotely logged to a machine hosting a VM cannot access its memory.

IV. THE PROPOSAL

A. An amicable entry into the cloud

We present some simple protocols to secure the VM launched by the user on the cloud and migration operations that could be brought about by a system administrator working for the cloud service provider.
This can even be put forth in a separate third party cloud server that would be an exclusive storage abyss on the cloud. For the commercial use, that is the large scale data exchange between parties, we suggest this server to be hosted at a location of the client who is authoritative enough to access all the collected data. Either ways, when launching a VM, it is to be made mandatory that

1) The VM is launched on a trusted node, and
2) The system administrator is unable to inspect or tamper with the initial VM state as it traverses the path between the user and the node hosting the VM.

The initial VM state can contain the **VM I**mage **(**VMI**)** (that can be personalized and contain secret data) and the user's public key (used for the login). In practice, the user can decide to use a VMI provided by the IAAS. That is he can choose an image from among a list provided by the service he opts for on the cloud. The protocol is designed on the fact that, before launching the VM, a user does not know which physical node the VM will be assigned unless it is the commercial organizations head if he has opted for the server to be hosted at his known location, and, among the components of the service, only trusts the cloud service provider.

B. The prudent tool for storage

One major benevolence in cloud computing is the property of AAA - Anything, Anywhere, Anytime. This has in turn rendered cloud computing as one of the most important facets of technological development. Here dealing with the storage provisions on the cloud alone, we look into an effective means of storage that overcomes all the negatives depicted above.
Considering the dropbox cloud storage facility that allows users to store date that automatically gets updated on all his systems that he initially registered is dire. The user may be accessing his data including videos, files, music from one system but it would be updated on all his VMs. This serves to be abysmal because any one accessing one of his registered systems may corrupt, hack or eat u the data. In addition to this, the depicted problem of the VM not belonging to the safe perimeter range also comes into light. Also the fact that the data is entrusted with the service provider provokes us to think if our data is actually safe. The same is the case with Amazon that provides 5gb data storage with practically no security to the user. (stated explicitly by them in their terms and conditions). In addition the music apps and SaaS puts amazon into darkness. The user not only has to worry about the system administrator eating up his data but in addition is forced to worry about other malicious users who have the potential ability to hack into another's cloud account and play havoc.
To overcome these fears and insecurities we propose a third party server system that exists on the cloud as visible to a normal viewers eye but ensures full privacy by :

1. Ensuring that the users Virtual Memory storage lies well within the safe perimeter ranges in the IAAS platform.

2. Edifying the users to launch their Virtual memory initially onto the cloud from only one trusted node.
3. Exalting and ensuring the main client with the server hosted at his required location if he has opted for one.

These can be in turn put to effect on a platform (Iaas) where a third party server on the cloud provides exclusive storage on payable terms rather than offering other services that include SaaS and PaaS. This would ensure that no malicious user gets to view or even come across another user. Moreover, this proposed third party server would provide the user with a separate login id and a password with double protection that includes

1. Identification of an image given forth by the user in the login screen
2. Audio track that would re confirm that the user is actually an authenticated one.

This would not only ensure that the user is authenticated but also ensures that no other user can even have a vague idea about the login id or even the existence of another user's VM.
Further, a message passing system can be established Like a mailing chat message service where the user gets updates on his cell phone from our proposed third party server whenever any update or retrieval is made from his/her virtual machine. This is similar to the online banking system that prevails ensuring and providing the users with the notion that their data are actually protected like currency. This proposal thereby

1. Eliminates the fear of insecurity prevailing in the existing storage systems on the cloud.
2. Provides not one or two but a triple confirmation and a three layer security to the user data on his/her VM.

V. AN AUGMENTATION THAT CAN AID THE GOVERNMENT.

The proposal of a third party server on the cloud ensuring triple security as depicted above can be deployed for the betterment and ease of the health sector of our nation .Since every user gets a separate storage space on the cloud with a login & password and security is immense with three layers as proposed earlier, this can be extended to meet the needs of the health sector of our nation.

With technological development at its peak it is high time to move on to the digital world. Today, hospitals, morgues mostly establish communication with the state government either by manual means where a representative from the hospital in case of birth, or the family member of the deceased in case of death have to manually go and approach the state government for birth or death certificates respectively. Even if its digital, it is through attachments in emails directed to the state government's website from a particular hospitals website or a private website. This can at times get clogged, reach the state government at its own pace (depending on the websites state). Further, security is a big question. As the data is being sent though mail, the sender might be worrying about his data being interrupted on its way and the time the government takes for its perusal. And in case of manual means, it is futile and naïve to travel, wait and get the work done. To overcome all this, we propose our third party server to be launched as follows.

Extending the proposal to the health sector would simply mean that every hospital approved by the government would get a user login id and can set a password. The triple layer of security would be ensured. Every hospital could update their

functioning that would include births, deaths, patients diagnosed with blighting diseased like leprosy, aids, cancer (including the form), accidents, etc. , number of patients in the ICU, ED and outpatients along with the treatment they are undertaking, the patients PHR (Personal Health Record) with necessary proof can be uploaded onto the cloud storage provided to the hospitals through its cloud account. Also the instruments used, developments in medicine, new technologies adopted can be included. This way, every hospital registered with the government of India would update their data on the cloud storage space.

All this data would be directed to the storage space provided to the government on the cloud. The top notch government officials registered alone get to view this collected data which is a pool of data that came from different hospitals across the nation by means of which the government can make its records lucidly.

The most impressing thing is that the main server would be hosted at the location of the ministry of health and family affairs or the IMA (Indian Medical Association). This would mean that the government needn't trust anyone with the data. This eliminates the fear of the system administrator breaking into the data and so on. This proposal can also be extended in terms of defense, census and so on. In case of the latter, the government workers no longer would have to go door
by door to collect census. Cloud on the whole would eliminate existing problems of data accumulation and would result in a highly digitalized world !

VI. CONCLUSIONS

In this paper, we put forward that concerns about the confidentiality and integrity of their data and computation are a major deterrent for enterprises looking to embrace cloud computing. We propose the design of a *trusted cloud computing platform* - a third party server on the cloud that would ensure full security to the user and guarantees genuine candor. This proposal of ours can also be applied to existing IaaS services such as Amazon , dropbox and enable them to

provide a closed box execution environment. This notion of ours guarantees confidential execution of guest VMs, and allows users to attest to the IaaS provider and determine if the service is secure before they launch their VMs. This proposal can be mould into a fully functional prototype where security as well as privacy would be provided at one go not only for private cloud users but also for the various sectors of the Government for their enhanced functioning.

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PERFORMANCE ANALYSIS OF MEDICAL IMAGE ATERMARKING ALGORITHMS IN FREQUENCY DOMAIN

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Abstract- Watermarking algorithms are used for embedding watermark like patient's history and doctor's signature in binary image format into host's medical image for telemedicine applications. This paper presents a comparative analysis of applying the watermark on DCT and DWT domain for medical images and the performance is analyzed based on PSNR and mean square error. It is found that DWT performs better than that of DCT algorithms.

Keywords: *Watermark, DWT, DCT, PSNR, mean square error, alpha.*

I.INTRODUCTION

The Institution of Medicine defines telemedicine as the use of electronic information technologies to provide and support health care when distance separates the participants. The most common application today is in the transmission of high resolution X-rays, cardiology, orthopedics, dermatology and psychiatry. Telemedicine arose originally to serve rural populations or any people who are geographically isolated, where time and cost of travel make access to the best medical care difficult. Now it is increasingly being used in mainstream medicine, to allow doctors the world over to share expensive recourses and valuable experience. Hence, healthcare industry demands secure, robust and more information hiding techniques promising strict secured authentication and communication through internet or mobile phones.

Medical image watermarking requires extreme care when embedding additional data within the medical images because the additional information must not affect the image quality as this may cause a misdiagnosis [7].This kind of a system requires a high level of security, which can be ensured by using digital watermarking techniques. This imposes three mandatory characteristics: robustness imperceptibility and capacity. There are different methods that has been using for medical image watermarking. The watermark can directly be embedded in the LSB as described by Mohamed Ali et al [13] [7]. In some applications it is often not allowed to alter
the image contents even one bit of information. The requirement of imperceptibility can be satisfied by two methods (1) by selecting region of non interest (RONI) watermarking which embeds the watermark information in RONI and keeping the region of interest (ROI) distortion free, and (2) by selecting reversible watermarking method which recover the original cover image by undoing the watermark embedding process at the receiving end after the image verification process is completed [3] [12].

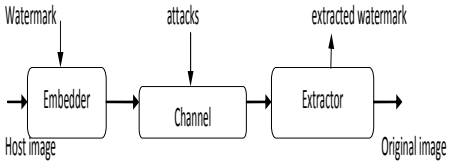

Fig. 1 A generic watermarking system model

In this generic watermarking model shown in Fig.1, there is a watermark embedder which embeds the information that is to be hidden (the watermark) in the original image (cover image) and the watermarked image is sent through the channel where there is a large probability of attacks such as removal attack, geometric attacks, cryptographic attacks, protocol attacks. At the receiver side there is an extractor which extracts the watermark from the stego image.

Digital image watermark techniques can also be classified based on the type of information needed in the extraction process. Using this classification criterion, it can be classified into two categories; non-blind and blind watermarking. A non-blind watermarking system requires the host image and the watermarked image in order to detect and extract the watermark data, but on the other hand, a blind watermarking system requires nothing other than the watermarked image itself to complete the process. In dealing with watermarking of medical images, some important constraints need to be satisfied. When watermark is embedded in the host image, it generates distortion. This distortion is highly undesirable in medical applications, whereby, even a small distortion in the images such as MRI and X-ray images might affect the decision of a physician. For this reason, it is necessary not only to extract the watermark but also to restore the original image completely. Reversible watermarking fulfills this requirement. It can restore the exact state of the original image. Whereas non reversible watermarking algorithms do not provide the exact reconstruction of the image

II. PROPERTIES OF MEDICAL IMAGE WATERMARKING

Security of medical information, derived from strict ethics and governmental rules, gives rights to the patient and duties to the health professionals. This imposes three compulsory characteristics: robustness, imperceptibility, capacity. Robustness is defined as the ability of watermark to resist against both lawful and illicit attacks. One of the stringent requirements of the image watermarking is the imperceptibility. Imperceptibility means that watermark embedded in the image must be invisible to the human eye. In watermarking of medical images, all the information necessary for physician such as identification of patient, diagnosis report, origin identification (who created the image) are embedded. This information is further increased when the image is sent to other physician for second opinion. Therefore, capacity for embedding the payload must be high.

Based on the domain in which the watermark can be embedded, the watermarking techniques are classified into 2 categories: spatial domain techniques and transform domain techniques. The most clear-cut way to hide the watermark within the cover content is to directly embed it in the spatial domain. There is number of advantages for using spatial domain watermarking. One advantage is temporal or spatial localization of the embedded data can automatically be achieved if the watermarked content undergoes some attacks and distortions are introduced in the watermarked content. Another advantage of spatial domain watermarking is that, an exact control on the maximum difference between the original and watermarked content is possible which allows the design of near-lossless watermarking systems, as required by certain applications such as protection of sensing or medical images. The oldest and the most common used method in this category is the insertion of watermark in the least significant bit of the pixel data [1][13]. Since the modification of the pixel data takes place in the LSB it is not visually perceptible. To obtain better imperceptibility as well as robustness, watermarking is done in frequency domain. The frequency domain watermarking techniques are also called multiplicative watermarking techniques. Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT)[13], Discrete Wavelet Transform (DWT) [5] is the most popular transforms operating in the frequency domain etc then the transform domain coefficients are modified by the watermark, [1][10]. The inverse transform is finally applied in order to obtain the watermarked image. Due to complicated calculations of forward and inverse transform the spatial domain techniques are less prone to attacks.

III. PERFORMANCE EVALUATION PARAMETERS

For evaluation of the watermarking algorithm, many criteria's are used. The most important among them are the quality of the image and the robustness of the watermarking scheme against various attacks.
Signal to noise ratio and peak signal to noise ratio

Among the most important distorting measures in image processing is the Signal to Noise Ratio (SNR) and the Peak Signal to Noise Ratio (PSNR).The SNR and the PSNR are respectively defined by the following formulas:

$$SNR = 10\log_{10}\left\{\left[\sum_{i,j}\frac{I^2(i,j)}{\sum_{i,j}[I(i,j)-K(i,j)]^2}\right]\right\} \quad (1)$$

$$\text{PSNR} = 20\log_{10}\left(\frac{\text{MAX}}{\text{MSE}}\right) \quad (2)$$

MAX is the maximum pixel value in the image where MSE is given by,

$$\text{MSE} = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}[I(i,j) - K(i,j)]^2 \quad (3)$$

where I (i, j) and K (i, j) are original and watermarked image respectively.

IV METHODOLOGY

A medical image 512×512 is taken as the test image; doctor's signature 60×100 is taken as the watermark. The watermark is embedded in the spatial domain. Here DCT and DWT domains are considered. The watermark is first applied in the DCT and DWT domain and the performance is evaluated based on PSNR and MSE. Fig.2 and Fig.3 represents the original and watermark that is used in this work. For wavelet transform first level decomposition is used and the mother wavelet used is haar wavelet.

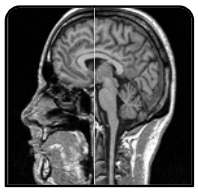

Fig .2 original image

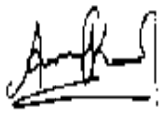

Fig.3 watermark

V EXPERIMENTAL RESULTS

The results after applying the watermark in DCT_8bit, DCT_16bit and DWT_8bit are analyzed and are given in Table 1, Table 2, and Table 3.

Table 1 shows the PSNR comparison of original and the watermarked image. From table it is seen that the performance of DCT_16 bit is better than DCT_8bit and DWT_8bit outperforms both DCT_8bit and DCT_16bit for different alpha values,

where alpha is the depth or weighing factor for the watermark.

Table 1 PSNR of original and watermarked image

Alpha	PSNR(original and watermarked image)		
	DCT_8bit	DCT_16bit	DWT_6bit
1	80.15	81.161	Infinity
2	67.728	67.759	121.283
3	60.157	60.102	117.234
4	56.726	56.692	109.710
5	54.031	54.047	107.802

As the alpha value increases the PSNR value is getting reduced i.e. the quality of the image is getting reduced. In the case of DWT it is seen that the PSNR value is not that much reduced.

Table 2 PSNR of original and retrieved signature

Alpha	PSNR(original signature and retrieved signature)		
	DCT_8bit	DCT_16bit	DWT_8bit
1	19.685	infinity	Infinity
2	39.120	infinity	Infinity
3	57.550	infinity	Infinity
4	11.389	47.676	Infinity
5	7.870	38.252	Infinity

Table 2 shows the PSNR value of the retrieved signature. The performance of DCT_8bit is poor when compared to DCT_16bit and DWT_8bit. The original signature can be retrieved for all alpha values changing from 1 to 5 in the case of DWT whereas the signature can be retrieved without error only when the alpha values are 1, 2, and 3 in the case of DCT_16bit. For values alpha=4 and alpha = 5 the image quality is reduced. The original signature cannot be reconstructed in the case of DCT_8bit for different values of alpha.

Fig 4, Fig 5 and Fig 6 shows the retrieved watermark from DCT_8bit, DCT-16bit and DWT_8bit respectively. It is clear from the images that the watermark can be retrieved perfectly from DWT domain

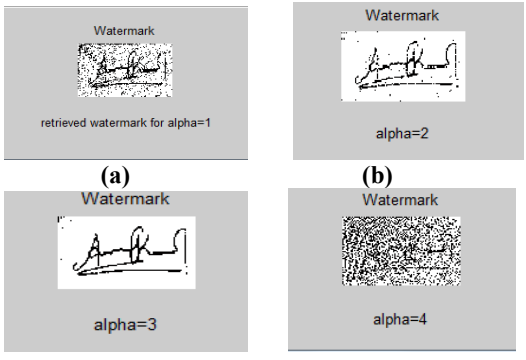

Fig. 4 Retrieved signatures after the removal of watermark from DCT_8bit domain for different values of alpha **(a)** alpha=1**(b)** alpha=2 **(c)** alpha=3 **(d)** alpha =4

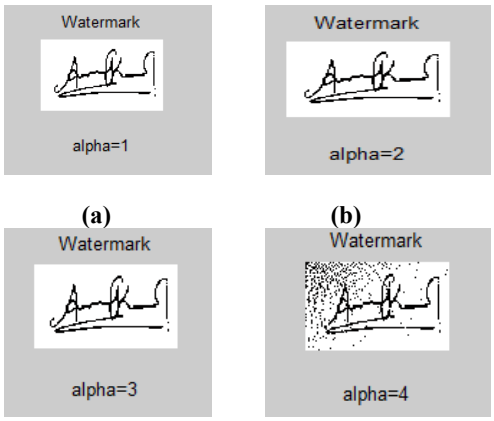

Fig .5 Retrieved signatures after the removal of watermark from DCT_16bit domain for different values of alpha **(a)** alpha=1**(b)** alpha=2 **(c)** alpha=3 **(d)** alpha =4

For DCT_8bit it is inferred from the Fig .4 that, for alpha = 3 we can retrieve the watermark with PSNR value 57.55. In the case of DCT_16bit it is seen that for alpha values 1,2 and 3 we can retrieve the watermark with PSNR values infinity that is the original watermark is perfectly reconstructed. For DWT_8bit the watermark can be retrieved perfectly for all values of alpha.

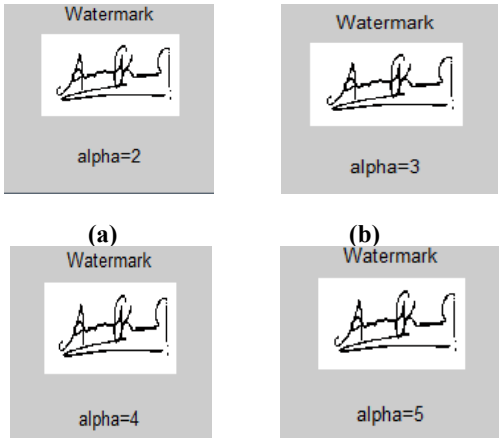

Fig .6 Retrieved signatures after the removal of watermark from DWT_8bit domain for different values of alpha **(a)** alpha=1**(b)** alpha=2 **(c)** alpha=3 **(d)** alpha = 4

Table 3 PSNR of original and watermarked image

Alpha	PSNR(original and retrieved image)

	DCT_8bit	DCT_16bit	DWT_8bit
1	146.329	Infinity	infinity
2	130.793	137.193	130.074
3	121.683	125.624	127.968
4	85.571	85.625	115.971
5	59.684	59.680	115.003

Table 3 shows the PSNR variation of the original and reconstructed image. From the Table 3 it is clear that the image quality is high for DWT when compared to DCT MSE is calculated for the different watermarking methods, it is found that the mean square error will be less for DWT as compared to DCT_8bit, DCT_16bit i.e. the Fig. 7, 8 and 9 shows the MSE of DCT_8bit, DCT_16bit and DWT_8bit

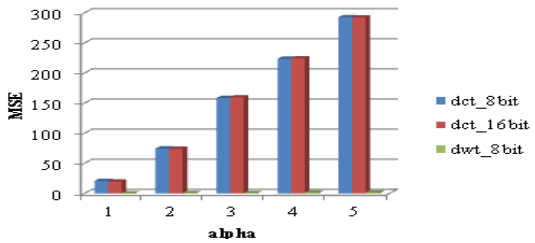

Fig .7 MSE comparison of original and watermarked image

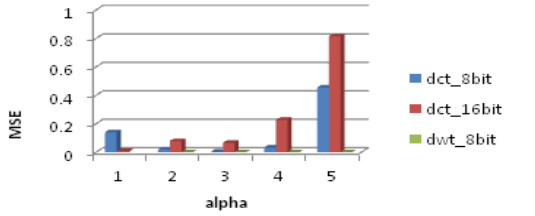

Fig .8 MSE comparisons of original signature and retrieved signature

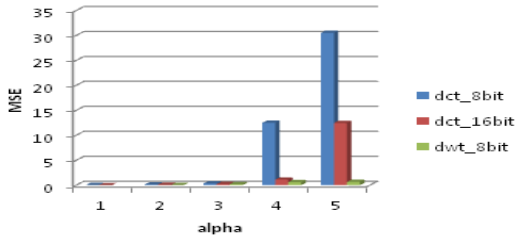

Fig .9 MSE comparisons of original and reconstructed image

VI. CONCLUSION

The philosophy, methodology, and characteristics of watermarking algorithms are given in detail in this paper. The performance evaluation of embedding the watermark in DCT and DWT domains is analyzed taking PSNR and MSE as the evaluation parameters. It is found that DWT performs quite better than DCT. The future work has to be extended by taking different size of watermark and to evaluate the robustness of the watermarking algorithm against different types of attacks.

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PERFORMANCE COMPARISON ON MEDICAL IMAGE SEGMENTATION ALGORITHMS

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Abstract- Image segmentation plays a crucial role in many medical-imaging applications, by automating or facilitating the delineation of anatomical structures and other regions of interest. In this paper explaining current segmentation approaches in medical image segmentation and then reviewed with an emphasis on the advantages and disadvantages of these methods and showing the implemented outcomes of the thresholding, clustering, region growing segmentation algorithm for the brain MRI and also explaining the edge detection of retinal image.

Key words- *Image segmentation, thresholding, clustering, region growing, edge detection.*

I. INTRODUCTION

Medical imaging is a valuable tool in medicine. Computed Tomography(CT), Magnetic Resonance Imaging(MRI), Ultra Sound imaging(US) and other imaging techniques provide more effective information about the anatomy of the human body. These technologies become more critical in diagnosis and treatment planning. Some computer algorithms are applying for the description of anatomical structures and other regions of interest are becoming increasingly important in assisting and automating specific radiological tasks. These algorithms, called image segmentation algorithms, play a vital role in numerous biomedical-imaging applications, such as study anatomical structure, Identify Region of Interest i.e. locate tumour and other abnormalities, Measure tissue volume to measure growth of tumour (also decrease in size of tumour with treatment), Help in treatment planning prior to radiation therapy; in radiation dose calculation [1].

Segmentation is the process of partitioning an image into multiple segments. The segmentation is to simplify and/or change the representation of an image into other form that is more significant and easier to analyse.

Even though a number of algorithms have been proposed in the field of medical image segmentation, medical image segmentation continues to be a complex and challenging problem. At present, various methods using are, Thresholding, Clustering methods Compression-based methods, Histogram-based methods, Edge detection, Region-growing methods, Split-and-merge methods, Partial differential equation-based methods, Graph partitioning methods, Watershed transformation, Model based segmentation Multi-scale segmentation, Neural networks segmentation [1].

This paper is organized as follows. Section II describes the widely using image segmentation algorithms, Section III discuss the experimental results of various segmentation algorithms. In Section IV, validation parameter to be considered is explained. In Section V conclusion of paper is discussed.

II. IMAGE SEGMENTATION ALGORITHMS

A. Thresholding

Thresholding is the simplest method of image segmentation. This method is based on a threshold value to turn a gray-scale image into a binary image [2]. In this method image is segmenting by comparing pixel values with the predefined threshold limit L [3].The following equation defining the threshold level.

Let X(i,j) be an image

$$X(i,j) = \begin{cases} 0, n(i,j) < L \\ 1, n(i,j) \geq L \end{cases} \quad (1)$$

where n(i,j) is the pixel value at the position (i,j). Thresholding is called adaptive thresholding when a different threshold is used for different regions in the image [4]. thresholding methods can be classified into the following six groups based on the algorithm manipulation . Histogram shape-based methods, clustering-based methods, entropy-based methods, object attribute-based methods, spatial methods, local methods.

B. Clustering method

This is an iterative technique that is used to partition an image into clusters. procedure of clustering method is explained in fig. 1.

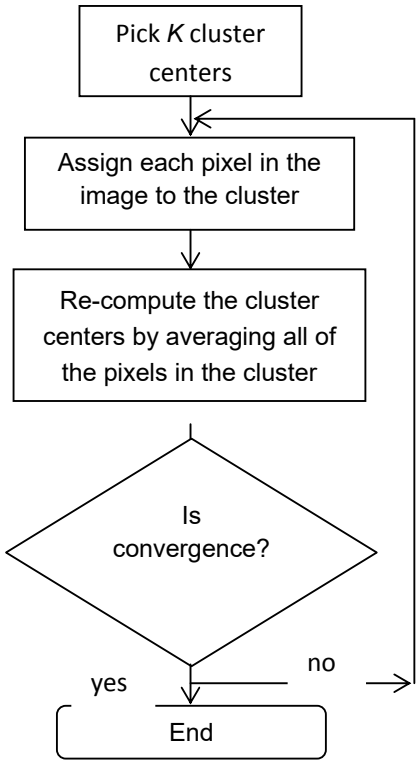


Fig.1. Flow chart showing computation of clustering method.

Clusters can be selected manually, randomly, or based on some conditions. distance between the pixel and cluster center is calculated by the squared or absolute difference between a pixel and a cluster center. The difference is typically based on pixel colour, intensity, texture, and location, or a weighted combination of these factors. More commonly used clustering algorithms are K – means algorithm, fuzzy c-means algorithm, expectation – maximization (EM) algorithm [1].

The quality of the final result of the clustering method depends mainly on the initial set of clusters. Since the algorithm is extremely fast, a collective method is to run the algorithm several times and select the best clustering. A drawback of the clustering algorithm is that the number of clusters k is an input parameter. A wrong choice of k may yield poor results. The algorithm also assumes that the variance is an appropriate measure of cluster scatter.

C. Compression – based method

Compression based method is an optimum segmentation method, because this is the one that minimizes the coding length of the data over all other possible segmentation techniques [5]. The relationship between compression and segmentation is that, segmentation tries to find patterns in an image and any regularity in the image can be used to compress it. And this method describes each segment by its texture and boundary shape. Each of these components is modelled by a probability distribution function [6].

This method yields the number of bits required to encode that image based on the given segmentation. Thus, among all possible segmentations of an image, this segmentation procedure produces the shortest coding length.

This can be achieved by a simple agglomerative clustering method. The distortion in the lossy compression determines the unevenness of the segmentation and its optimal value may differ for each image. This parameter can be estimated heuristically from the contrast of textures in an image.

D. Histogram – based method

In this method, a histogram is computed from all of the pixels in the image, and the peaks and valleys in the histogram are used to locate the clusters in the image [4].Colour or intensity can be used as the parameters for the measure. Since the histogram-based methods are very efficient when compared to other image segmentation methods because they typically require only one pass through the pixels.

In mathematical sense, a histogram is a function X_i that counts the number of observations that fall into each of the disjoint categories which is known as *bins*, whereas the graph of a histogram is merely one way to represent a histogram. Thus, if we let N be the total number of observations and l be the total number of bins, the histogram X_i meets the following conditions (Karl Pearson):

$$N = \sum_{j=1}^{l} X_j \qquad (2)$$

An improvement can be made in this technique by recursively apply the histogram method to every clusters in the image in order to divide image into smaller clusters [7], [8]. This is repeating until no more clusters are formed. One disadvantage of the histogram-seeking method is that it may be difficult to identify significant peaks and valleys in the image [4].

Histogram-based approaches can also be quickly applicable over multiple frames, while maintaining their single pass efficiency. The same approach that is done with single frame can be applied to multiple frame, and after the results are merged, peaks and valleys that were previously difficult to identify are more likely to be distinguishable. The histogram based method can also be applied on a per pixel level, and the information result are used to determine the most frequent colour for the pixel location.

E. Edge detection

The edge-based approaches is to detect the object boundaries by using an edge detection operator and then extract boundaries by using the edge information [9]. The problem of edge detection is the presence of noise that results in random variation in level from pixel to pixel. Therefore, the ideal edges are never encountered in real images because of noise [9]. A great diversity of edge detection algorithms have been devised with differences in their mathematical and algorithmic proper-ties such as Roberts, Sobel, Prewitt, Laplacian, and Canny, all of which are based on the difference of gray levels [9]. The difference of gray levels can be used to detect the discontinuity of gray levels.

Although many algorithms for boundary detection have been developed to achieve good performance in field of image processing, most algorithms for detecting the correct boundaries of objects have difficulties in medical images in which ill-defined edges are encountered [9]. Medical images are often noisy and too complex to expect local, low level operations to generate perfect primitives. The complexity of medical images makes the correct boundary detection very difficult.

F. Region-growing method

The region growing is a mostly used classical segmentation method. These region growing based segmentation models shares the following assumption about the image pixel properties [3].The intensity values within each region/object conforms to Gaussian distribution, The mean intensity value for each region/object is different.

Region growing is a technique for extracting an image region that is connected based on some predefined criteria. These criteria can be based on intensity information and/or edges in the image [1]. One example for the region growing method is seeded region growing. The procedure for the same as follows:

1. This method takes a set of seeds as input along with the image.
2. The seeds mark each of the objects to be segmented.
3. The regions are iteratively grown by comparing all unallocated neighbouring pixels to the regions.
4. The difference between a pixel's intensity value and the region's mean, δ, is used as a measure of similarity.
5. The pixel with the smallest difference measured this way is allocated to the respective region.
6. This process continues until all pixels are allocated to a region.

The primary disadvantage of region growing is that it requires manual interaction to obtain the seed point. Split-and-merge is an algorithm related to region growing, but it does not require a seed point. Region growing can also be sensitive to noise, causing extracted regions to have holes.

G. Split and merge method

Split and merge method also called as quad - tree segmentation, because split-and-merge segmentation is based on a quad-tree partition of an image. The process of split and merge segmentation method is explained as follow in fig. 2:

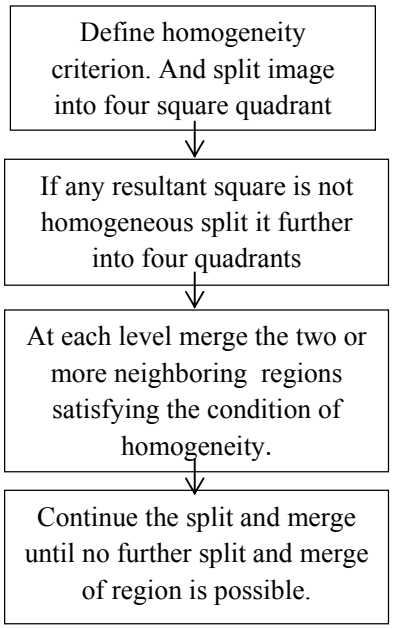


Fig.2. The flowchart of split and merge method.

This is the combination of splits and merges utilizing the advantage of the two methods. This method starts at the root of the tree that represents the whole image. If it is found non-uniform (not homogeneous), then it is split into four son-squares (the splitting process), and so on so forth. Conversely, if four son-squares are homogeneous, they can be merged as several connected components (the merging process). The node in the tree is a segmented node. This process continues recursively until no further splits or merges are possible. When a special data structure is involved in the implementation of the algorithm of the method, its time complexity can reach $O(n\log n)$, an optimal algorithm of the method [1].

H. Graph partitioning methods

Graph partitioning methods can effectively be used for image segmentation. In these methods, the image is modelled as a weighted, undirected graph. Usually a pixel or a group of pixels are associated with nodes and edge weights define the (dis)similarity between the neighbourhood pixels. The graph (image) is then partitioned according to a

criterion designed to model "good" clusters. Each partition of the nodes (pixels) output from these algorithms are considered an object segment in the image. Some popular algorithms of this category are normalized cuts, random walker, minimum cut, isoperimetric partitioning, minimum spanning tree-based segmentation.

This graph partitioning algorithm is perfectly adapted to a volume binary classification issue [10]. Moreover, the transcription of a segmentation issue into an energy minimization framework makes it possible to encode various characteristics of the data: classification training, degree of similarity between voxels of the same class (region-based approaches), changes between classes (boundary-based approaches), etc.

Once the graph is built, correct weight is assigned to each links according to some relevant cost functions, graph cuts algorithm, the regional term cost function is defined after an interactive process [10]. Histograms are built from this labelling and probability density functions are extracted for each class and encoded in the graph. Graph cut segmentation can be formulated as an energy minimization problem such that for a set of pixels P and a set of labels L, the goal is to find a labelling f: P→L that minimizes the energy function E(f) [10].

$$E(f) = \sum_{p \in P} R_p(f_p) + \sum_{p \in P, q \in N_p} B_{p,q}(f_p, f_q) \quad (3)$$

where N_p is the set of pixels in the neighbourhood of p, $R_p(f_p)$ is the cost of assigning label $f_p \in L$ to P, and $B_{p,q}(f_p,f_q)$ is the cost of assigning labels $f_p, f_q \in L$ to p and q.

I. Neural networks segmentation

Inspired by the way biological nervous systems such as human brains process information, an artificial neural network (ANN) is an information processing system which contains a large number of highly interconnected processing neurons [11]. These neurons work together in a distributed manner to learn from the input information, to coordinate internal processing, and to optimise its final output.

The basic structure of a neuron can be theoretically modelled as shown in fig. 3 where X $\{x_i, i = 1, 2, \ldots, n\}$ represent the inputs to the neuron and Y represents the output. Each input is multiplied by its weight w_i, a bias b is associated with each neuron and their sum goes through a transfer function f [11].

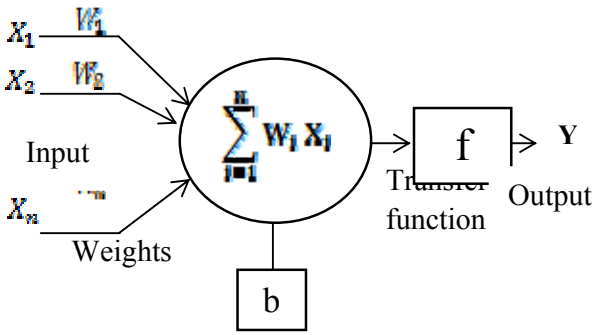


Fig.3. The model of neuron

Neural Network segmentation relies on processing small areas of an image using an artificial neural network or a set of neural network. There are several different neural network architectures available for medical imaging applications, Feed-forward Network, Radial Basis Function Networks, Feed-back Network, Self-Organising Map [11].

Each neuron in the network corresponds to one pixel in an input image, receiving its corresponding pixel's color information (e.g. intensity) as an external stimulus. Each neuron also connects with its neighboring neurons, receiving local stimuli from them. The external and local stimuli are combined in an internal activation system, which accumulates the stimuli until it exceeds a dynamic threshold, resulting in a pulse output. Through iterative computation, pulse coupled neural network. neurons produce temporal series of pulse outputs. The temporal series of pulse outputs contain information of input images and can be utilized for various image processing applications, such as image segmentation and feature generation.

J. Shortcomings of Segmentation Methods

Segmentation of medical images is a difficult task as medical images are complex in nature and rarely have any simple linear feature. Further, the output of segmentation algorithm is affected due to, Partial volume effect, Intensity inhomogeneity, Presence of artifacts, Closeness in gray level of different soft tissue.

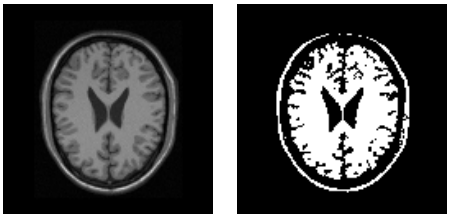
Medical images are often noisy and too complex to expect local, low level operations to generate perfect primitives. Medical imaging technique like ultra sound, CT may contain echo perturbations and speckle noise, it may affect the segmentation.

III. EXPERIMENTAL RESULTS

In this section discussing the implementation of various segmentation algorithms for the MRI of brain, And edge detection of retinal image.

A. Thresholding

This method is based on threshold value.

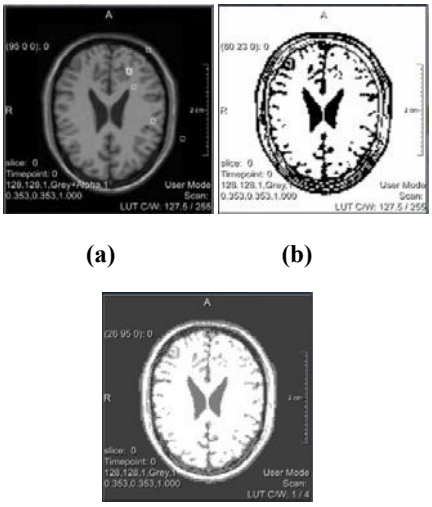


(a) **(b)**

Fig .4**.** Segmentation of brain MRI using thresholding. (a) original (b) segmented image

This best segmentation obtained for the threshold value 0.384. Selection of threshold value should be correct otherwise output will not be a good segmented one.

B. Clustering method



(a) **(b)**

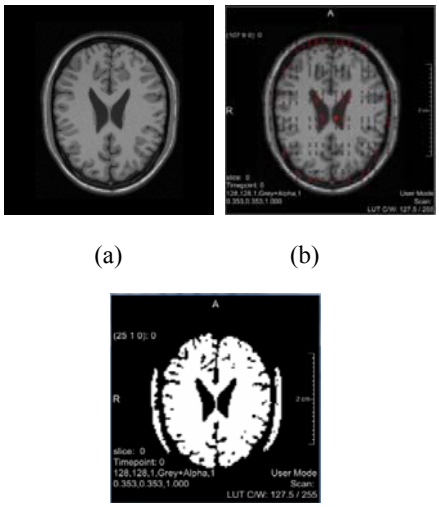
(c)

Fig.5. Clustering segmentation method.(a) original image,(b) and (c) segmented output

In this example value of cluster center 3.8057,Iterartion limit given is 1000, and number of iterations performed is 4.

C. Region-growing method

Region growing is a technique for extracting an image region that is connected based on some predefined criteria. These criteria can be based on intensity information and/or edges in the image. The seeds mark each of the objects to be segmented. The primary disadvantage of region growing is that it requires manual interaction to obtain the seed point.



(a) (b)

(c)

Fig.6. Region growing segmentation. (a)original image, (b) image with seed points, (c) segmented image.

D. Edge detection

Due to the presence of intensity inhomogeneity and closeness in gray level of different tissue, edge detection cannot be done in MRI brain image [1].

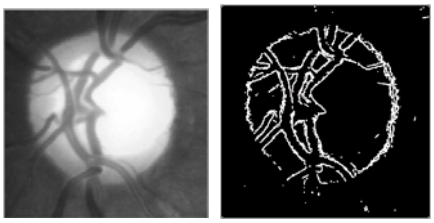


Fig.7. Edge detection operation

The difference of gray levels can be used to detect the discontinuity of gray levels.which is used to detect the object boundary.

IV. VALIDATION

To quantify the performance of a segmentation method, validation experiments are necessary. The most straightforward approach to validation is to compare the automated segmentations with manually obtained segmentations. other common approach to validating segmentation methods is through the use of physical phantoms or computational phantoms. Specificity, sensitivity, and accuracy are the other parameters to be considered.

V. CONCLUSION

Image segmentation plays a crucial role in many medical-imaging applications, by automating or facilitating the delineation of anatomical

structures and other regions of interest. Many methods are existing and still developing the new methods for the segmentation to overcome the shortcomings of the existing methods. Here various segmentation methods have implemented on brain MRI and edge detection on retinal image. Outcomes are depend on some input parameter like, threshold for the thresholding, number of cluster centres, and seed point for the region growing method. Region growing needs manual interaction. Running time for the clustering method depends on the number of iteration used. Edge detection depends on discontinuity of gray level and on intensity variation on the gray scale images. Above explained methods are gives almost identical outcomes, when the inputs are accurate.

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COMPARATIVE STUDY OF MULTIPLE INPUT CONVERTERS

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Abstract- A new three-input dc–dc boost converter is proposed in this paper. The proposed converter interfaces two unidirectional input power ports and a bidirectional port for a storage element in a unified structure. This converter is interesting for hybridizing alternative energy sources such as photovoltaic (PV) source, fuel cell (FC) source, and battery. Supplying the output load, charging or discharging the battery can be made by the PV and the FC power sources individually or simultaneously. The proposed structure utilizes only four power switches that are independently controlled with four different duty ratios. Utilizing these duty ratios, tracking the maximum power of the PV source, setting the FC power, controlling the battery power, and regulating the output voltage are provided. In order to validate the performance of the converter, different approaches along with their advantages & disadvantages are discussed in this paper.

INTRODUCTION

Nowadays, photovoltaic (PV) energy appears quite attractive for electricity generation because of its noiseless,pollution-free, scale flexibility, and little maintenance. Because of the PV power generation dependence on sun irradiation level,
ambient temperature, and unpredictable shadows, a PV-based power system should be supplemented by other alternative energy sources to ensure a reliable power supply. Fuel cells (FCs)are emerging as a promising supplementary power sources due to their merits of cleanness, high efficiency, and high reliability.
Because of long startup period and slow dynamic response weak points of FCs ,mismatch power between the load and the FC must be managed by an energy storage system. Batteries are usually taken as storage mechanisms for smoothing output power, improving startup transitions and dynamic characteristics,and enhancing the peak power capacity .Combining
such energy sources introduces a PV/FC/battery hybrid power system. In comparison with single-sourced systems, the hybridpower systems have the potential to provide high quality, more reliable, and efficient power. In these systems with a storage element,the bidirectional power flow capability is a key feature at the storage port. Further, the input power sources should have the ability of supplying the load individually and simultaneously.Many hybrid power systems with various power electronic converters have been proposed in the literature up to now.

This paper is organized as follows.Different types of converters along with their operations advantages & disadvantages are explained in Section I. The proposed converter is given in Section II.Section III concludes this paper.

1.1.Two-inputcurrent-fedfullbridgedc/dcconverter(2002)

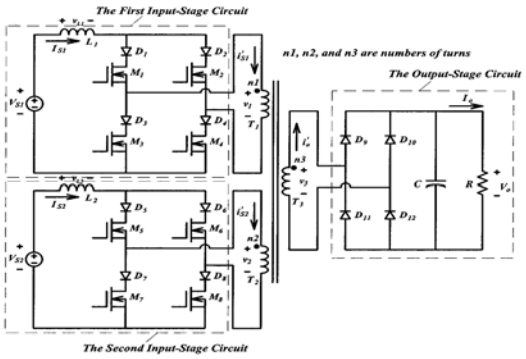

Fig 1: Circuit topology of the proposed two-input current-fed full-bridge dc/dc converter

The schematic diagram of the proposed two-input current-fed full-bridge dc/dc converter is shown in Fig. 1. It consists of two current-source input-stage circuits, a three-winding coupled transformer, and a common output-stage circuit. The number of the input-stage circuits can be increased to meet the practical multi-input dc sources requirement while the coupled transformer and the output-stage circuit remain unchanged. In order to produce the desired magnetic flux in the coupled magnetic core, the current source input-stage circuit is implemented by the current-fed full-bridge dc/ac converter. Each dc voltage source associated with a choke inductor becomes a dc current source, which implies that the amplitude of the dc voltage source can be different. This is a very important feature for the multi-input dc/dc converter since voltage variations of these dc sources could be significant. Each switch of the current-fed full-bridge dc/ac converter in the input-stage circuit should be in series with a reverse-blocking diode. The reverse-blocking diode can regulate the direction of the current flow and prevent the reverse power flow from other dc sources via the coupled transformer and switches' body diodes. Without these reverse-blocking diodes, different dc sources of the proposed multi-input dc/dc converter

cannot deliver power to the load simultaneously. Also, all input-stage windings and the output-stage winding of the coupled transformer should be wound on the same magnetic core to ensure that the total flux linkage produced by each input current source can entirely pass through the output-stage winding. The output-stage circuit is implemented by an ac/dc full-bridge rectifier with appropriate output filters.

1.1.1.Advantages & Disdvantages

It can be seen that the MOSFET is operated with ZCS at turn-off transition. In fact, all upper MOSFETs in each input-stage circuit of the proposed converter are operated with ZCS at turn-off transition with similar drain–source voltage and drain current wave forms .On the other hand, the simulated and measured waveforms of ZVS at turn-on transition are shown. Actually, all lower MOSFETs in each input-stage circuit of the proposed converter are operated with ZVS at turn-on transition. Noises appearing in voltage and current waveforms are caused by the parasitic elements of the switching devices and the transformer.

It can be shown that the transformer output current is the combination of the transformer input current and , which results from the concept of the magnetic flux additivity. It also illustrates that power can be delivered from these two voltage sources to the load individually and simultaneously. It can be seen that the proposed multi-input converter has the minimum efficiency of 84% for various operating conditions.These experimental results verify the performance of the proposed multi-input dc/dc converter with the phase-shifted PWM control.

1.2. Soft-switched bidirectional half-bridge dc–dc converter(2004)

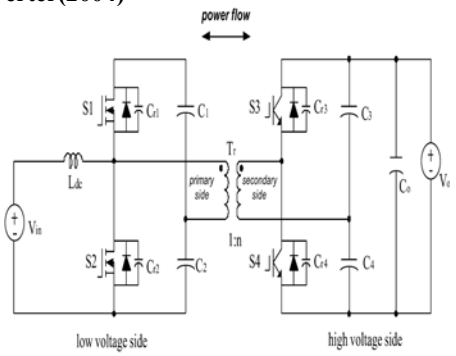

Fig 2.Soft-switched bidirectional half-bridge dc–dc converter

The bidirectional dc–dc converter for fuel cell applications is shown in fig.2. The circuit consists of an inductor on the battery side and two half-bridges each placed on each side of the main transformer . Each switching device has a small parallel capacitor for soft switching. When power flows from the low voltage side (LVS) to the high voltage side (HVS), the circuit works in boost mode to keep the HVS voltage at a desired high value. In the other direction of power flow, the circuit works in buck mode to recharge the battery from the fuel cell or from absorbing regenerated energy. The HVS switches are implemented with IGBTs, while the low voltage side switches are MOSFETs. The arrangement of the inductor and the LVS half bridge is unique. The LVS half bridge has double functions serving as

1) a boost converter to step up voltage;
2) an inverter to produce high frequency ac voltage.

The boost function is achieved by the inductor and the LVS half bridge. The LVS boost converter draws much smoother current from the load voltage source than full bridge voltage source inverter. This integrated double function provided by the LVS half bridge is advantageous over other topologies, because the primary current rating of the transformer and current stress of the LVS devices are minimized. The capacitor across each switch is a lossless snubber (or resonant capacitor) for soft switching. The transformer is used to provide isolation and voltage matching. The leakage inductance of the transformer is utilized as an interface and energy transfer element between the two voltage-source half bridge inverters: LVS and HVS half bridges. The amount of power transferred is determined by the phase shift of the two square-wave voltages. The current waveform is determined by the phase shift and voltage relationships .

1.2.1.Advantages & Disadvantages

A bidirectional dc-dc converter has been built to validate the soft switching analysis . Compared to a full bridge counterpart converter that was developed previously at the lab, the size of the converter is saved more than 1/3, which shows the high power density feature. The size saving was mainly from less current stress, less gate drive circuit, and higher efficiency (94% versus 92%). As described previously, the new converter has the same primary current rating of the transformer as the full bridge converter. The primary current of the transformer flows through only one MOSFET at any time instead of two in the full bridge converter. This resulted in a great efficiency improvement, because the conduction loss is a major power loss. The switching loss is minimized due to soft switching.

1.3.Multi-input inverter(2007)

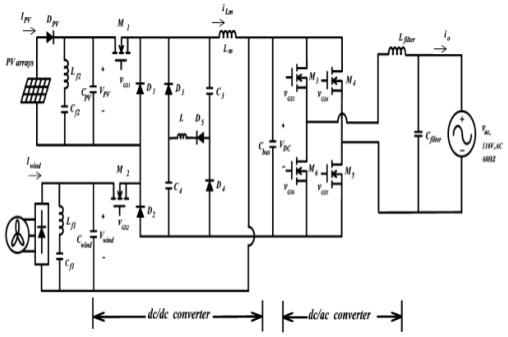

Fig 3.Schematic diagram of the proposed multi-input inverter

The proposed multi-input inverter is shown in fig 3. It consists of a buck/buck-boost fused multi input dc–dc converter and a full-bridge dc/ac inverter. The input voltage sources consist of PV array and the rectified wind turbine. By applying the pulse-with-modulation (PWM) control scheme with appropriate MPPT algorithm to the power switches and PV array,the multi-input dc–dc converter can draw maximum power from both the PV array and the wind turbine individually or simultaneously. The dc bus voltage will be regulated by the dc/ac inverter with sinusoidal PWM (SPWM) control to achieve the input output power-flow balance. Details of the operation principle for the proposed multi-input inverter are introduced as follows.

A. PV Array

The PV array is constructed by many series or parallel connected solar cells . Each solar cell is form by a semi conductor, which can produce currents by the photovoltaic effect. It can be seen that a maximum power point exists on each output power characteristic curve. Therefore, to utilize the maximum output power from the PV array, an appropriate control algorithm must be adopted

B. MPPT Algorithm

Different MPPT techniques have been developed.Among these techniques, the perturbation and observation (P&O) method with the merit of simplicity is used. The perturbation of the output power is achieved by periodically changing (either increasing or decreasing) the controlled output current. The objective of the P&O method is to determine the changing direction of the load current.At the beginning of the control scheme, the output voltage and output current of the source (either the PV array or the wind turbine) are measured, then the output power can be calculated.

C. Wind Turbine

Among various types of wind turbines, the permanent magnet synchronous wind turbine, which has higher reliability and efficiency, is preferred . It had been proven that the energy conversion efficiency, of the wind turbine is a function of the tip speed ratio, which is defined as value of it is only achieved at a particular tip speed ratio. Since the speed of the wind is not constant, the rotational speed of the wind turbine must be adjustable to ensure a constant tip speed ratio to gain the maximum . The output current change of the wind turbine will cause of the rotational speed as well as to change. Since is a function of , the output power of the wind turbine will change, too. Therefore, by controlling the output current of the wind turbine, the rotational speed of the wind turbine blades can be adjusted to achieve the appropriate tip speed ratio. Eventually, the maximum value of can be obtained and the maximum power can be transferred from the air stream to the wind turbine to produce the maximum electrical power. For the convenience of experiment, instead of natural wind, a controllable dc motor is used to drive the wind turbine to simulate the actual operation situation under the natural air-stream. When the output power of the wind turbine is small, the dc motor will request small power from the dc source to drive the wind turbine. When the output current of the wind turbine is increased, the output voltage and the rotational speed will be decreased. These curves have same characteristics with those driven by the natural air-stream. Each one of the curves represents a constant driving power from the dc motor. The output power of the wind turbine is drawn by an electronic load. The load current is gradually increased, and then the output power can be measured. Output power characteristic curves shown in Fig. 6 imply that the wind turbine will generate different maximum output power for different wind speed. Because the output power characteristic curves of the wind turbine are similar to those of the PV array shown in, the P&O method is adopted as the MPPT algorithm for the wind turbine. Therefore, a power electronic converter with appropriate controller is needed to process the wind energy which varies considerably according to the meteorological conditions such as wind speed.

D. Multi-Input DC–DC Converter

The proposed multi-input dc–dc converter is the fusion of the buck-boost and the buck converter . Syntheses of the multi input dc–dc converter are done by inserting the pulsating voltage source of the buck converter into the buck-boost converter. In order not to hamper the normal operation of the buck-boost converter and to utilize the inductor for the buck converter, the pulsating voltage source of the buck converter must be series-connected with the output inductor.If one of the voltage sources is failed, the other voltage can still provide the electric energy,.

1.3.1.Advantages & Disadvantages:

The PV array is formed by 24 series-connected solar panels while the Bergey BWC 1500 is used for the wind turbine. Each PV array has peak power of 60W and open voltage of 21V. The wind turbine is a three-phase permanent magnetic generator with rated power of 1.5 kW at rated wind speed of 12.5 m/s. It reveals that the multi-input dc–dc converter can deliver power from both of the two energy sources to the dc bus simultaneously. Output current of the PV array is then increased gradually because of the MPPT control algorithm with the P&Omethod. Eventually, the output power of the PV array will reach its maximum power point and stay around that place. The wind turbine is connected to the multi-input dc–dc converter . However, it shows that the MPPT feature for the PV arrays and the wind turbine are both achieved. The incoming power from the PV array or/and the wind turbine will cause the rise of the

dc bus voltage. The value of dc bus voltage is regulated by adjusting the amplitude of the ac output current. If the value of the dc bus voltage is higher than a pre-set range, then the ac output current of the dc/ac inverter will be increased in order to lower the dc bus voltage. On the contrary, if the dc bus voltage is smaller than the pre-set range, the amplitude of the ac output current must be reduced to boost up the dc bus voltage. Once the dc bus voltage reaches its pre-set range, the dc/ac inverter will begin to inject ac output current into the utility line. Since the input power is not a constant, a small variation of the ac output current amplitude can be found .

1.4 Feasible Topologies for Multiple-Input DC–DC Converters(2008)

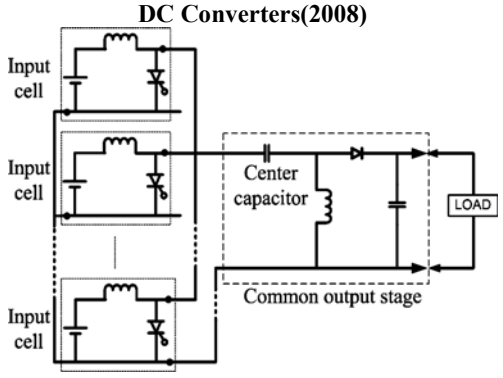

Fig.4 Feasible converter with center capacitor in the common output stage

Based on the analysis, it is possible to identify feasible and unfeasible topologies that can be expanded into MICs is shown in fig 4. Among the basic converter topologies—buck, boost, buck– boost and C′ uk only the buck and the buck–boost topologies are feasible because they are the only ones that use the only acceptable input cell. Both of these topologies have a current source interface that makes them suitable for any source technology , including those requiring a smooth current profile without the need for an additional input filter . The violation is the most common cause of unfeasibility, especially if the single-input converter has four switches. Some of these feasible configurations are cascades of two simpler topologies are feasible topologies with the addition of the current-source conditioning filter .The topologies with the addition of a current-source conditioning filter to a fundamental converter are D6 (buck) and F5 (buck–boost).

Other configurations, such as E5 (buck) and F6 (buck–boost), are basic topologies with additional filtering at the output. Finally, configurations E3 and F1 can be reduced to a buck–boost and a buck converter, respectively, because these topologies include redundant branches with inductors and capacitors. Thus only configurations A1 (buck), A5 (buck–boost), G1(1), and G6 are fundamental topologies suitable to be expanded into MICs.The configurations that can be expanded into MICs if the assumption of minimizing the total number of components is relaxed and the center capacitor is distributed from the common stage. Without loss of generality, only two input cells with input voltages *V*1 and *V*2 are considered, although a general input-to-output voltage relationship for the SEPIC, C′ uk, and MICs can be found. *D*1 and *D*2 represent the commanded duty cycles in input legs 1 and 2, respectively, whereas *D*2 ,eff is the portion of the switching period.

1.4.1.Advantage&Disadvantage

Certain rules have to be followed which makes added advantage . All feasible input cells must contain at least one independently controlled switch. This rule is derived from the condition requiring some degree of freedom in the control of the power delivered by each source. To meet the condition of independent control in each input, the connection of the input cells to the common stage should not lead to redundant switches, i.e., independent controlled switches in parallel. In the case that an MIC's single-input original topology has a center capacitor, such as in the single-ended primary inductance converter and the C′ uk converters, then the average voltage of the capacitor should not depend on the input voltage.

1.5High step-up bidirectional isolated converter(2009)

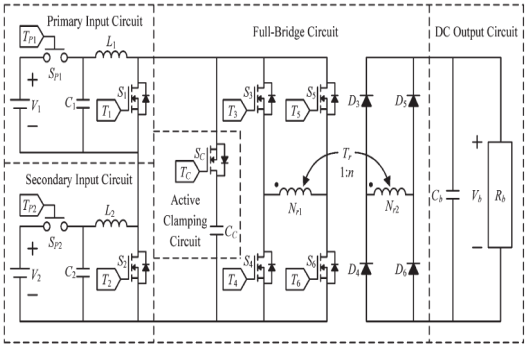

Fig.5 High step-up bidirectional isolated converter

1.5.1.Theory of operation

The topology of the proposed high step-up bidirectional isolated converter is shown in fig.5. It contains five parts, including a primary input circuit, a secondary input circuit, an active clamping circuit, a full-bridge circuit, and a dc output circuit. *V*1 denotes the primary dc input voltage. *V*2 exhibits the secondary dc input voltage, and this power source could be a rechargeable battery. *SP*1, *SP*2, *TP*1, and *TP*2 express the power on/off switches and their driving signals produced according to the power management. *C*1, *C*2, *L*1, and *L*2 represent the individual capacitors and inductors in the primary and secondary input circuits, respectively. *CC*, *SC*, and *TC* are the clamping circuit. *Si* and *Ti*(*i* = 1 □ 6) are the low-voltage side switches and their driving signals, which are generated bythe PWM. *Nr*1 and

*Nr*2 indicate the primary and secondary windings of a two-winding transformer (*Tr*) with a turns ratio of 1 : *n*. *Dj*(*j* = 3 □ 6) expresses the high-voltage side diodes for rectifying the secondary-winding current of the transformer (*Tr*) to the output capacitor (*Cb*). *Vb* and *Rb* describe the dc-bus voltage and load in the dc output circuit.*N*1 and *N*2 indicate the primary and secondary windings of the ideal transformer. The simplification has the following assumptions:
1) all circuit components have ideal characteristics; 2) the capacitors *C*1, *C*2, *CC*, and *Cb* are large enough so that the voltage ripples due to switching are negligible and could be taken as constant voltage sources *V*1, *V*2, *V*CC, and *V*dc; 3) the power on/off switches *SP*1 and *SP*2 are omitted; and 4) the magnetizing inductor is large enough so that it could be seen as a high impedance path to ignore. According to different power conditions, the operational states of the proposed converter can be divided into three states, including a stand-alone state with single input power source, a united power supply state with two input power sources, and a charge and discharge state with two input power sources.

1.5.3.Advantages&Disadvantages

In order to verify the effectiveness of the newly designed high step-up bidirectional isolated converter. Basically, the primary and secondary input powers have the same standing for different power sources. By considering the battery power requirement in the driving circuit, it is better to place the main power (e.g., FC) to the primary input power source and to place the battery to the secondary input power source because a common ground is easily obtained in this
placement. Moreover, two Pb–acid batteries in series connection with12 V/7 A · h are taken as the power storage mechanism for the secondary power source. In the experimentations, the bidirectional isolated converter is designed to operate from a variability dc input (*V*1 = 23 □ 28.6 V) with a battery stack (*V*2 = 24 V ± 10%) to deliver a constant output *V*dc = 400 V. For
solving the problem of the output voltage variance with different loads, the proposed converter with proportional–integral(PI) feedback control is utilized . Thus, the conservative selection is adopted for overcoming the possible occurrence of nonideal characteristics in the components. For ensuring that the duty cycles *d*1 and *d*2 should be greater than 0.5 at the worst case in the united power supply state, the theoretical duty cycles of switch, which are *d*1 = 0.58 and *d*2 = 0.61, are determined if the maximum input voltages are assumed to be *V*1 = 28.6 V and *V*2 = 26.4 V. The optimum values of the duty cycles *d*1 and *d*2 can be adjusted around the theoretical values according to the respective voltage and current PI controllers.

2.PROPOSED SYSTEM

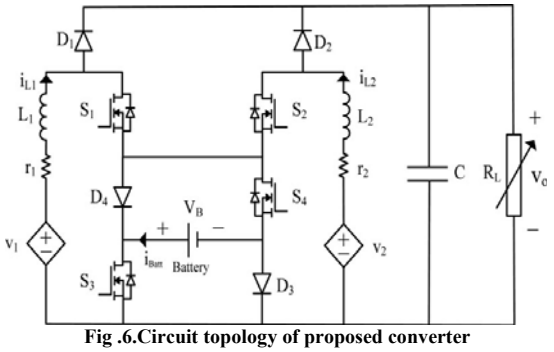

Fig .6.Circuit topology of proposed converter

The structure of the proposed three-input dc–dc boost converter is represented in Fig. 6. As seen from the figure, the converter interfaces two input power sources *v*1 and *v*2 , and a battery as the storage element. The proposed converter is suitable alternative for hybrid power systems of PV, FC, and wind sources. Therefore, *v*1 and *v*2 are shown as two dependent power sources that their output characteristics are determined by the type of input power sources. For example, for a PV source at the
first port, *v*1 is identified as a function of its current *iL* 1 , light intensity, and ambient temperature. In the converter structure, two inductors *L*1 and *L*2 make the input power ports as two currenttype sources, which result in drawing smooth dc currents from the input power sources. The *RL* is the load resistance, which can represent the equivalent power feeding an inverter. Four power switches *S*1 , *S*2 , *S*3 , and *S*4 in the converter structure are the main controllable elements that control the power flow of the hybrid power system. The circuit topology enables the switches to be independently controlled through four independent duty ratios *d*1 , *d*2 , *d*3 , and *d*4 , respectively. As like as the conventional boost converters, diodes *D*1 and *D*2 conduct in complementary manner with switches *S*1 and *S*2 . The converter structure shows that when switches *S*3 and *S*4 are turned ON,their corresponding diodes*D*3 and*D*4 are reversely biased by the battery voltage and then blocked. On the other hand, turn-OFF state of these switches makes diodes *D*3 and *D*4 able to conduct input currents *iL* 1 and *iL* 2 . In hybrid power system applications,the input power sources should be exploited in continuous current mode (CCM). For example, in the PV or FC systems, an important goal is to reach an acceptable current ripple in order to set their output power on desired value. Therefore, the current ripple of the input sources should be minimized to make an exact power balance among the input powers and the load.Therefore, in this paper, steady state and dynamic behavior of the converter have been investigated in CCM. In general, depending on utilization state of the battery, three power operation modes are defined to the proposed converter. These modes of operation are investigated

with the assumptions of utilizing the same sawtooth carrier waveform for all the switches, and $d3$,$d4$ <min ($d1$,$d2$) in battery charge or discharge mode. Although exceeding duty ratios $d3$ and $d4$ from $d1$ or $d2$ does not cause converter malfunction, it results in setting the battery power on the possiblemaximum values. In order to simplify the investigations, it is assumed that duty ratio $d1$ is less than duty ratio $d2$. Further, with the assumption of ideal switches, the steady-state equations are obtained in each operation mode.

3. CONCLUSION

A new three-input dc–dc boost converter with unified structure for hybrid power systems is proposed in this paper. The proposed converter is applied to hybridize a PV, an FC, and a battery storage system. Four independent duty ratios of the converter facilitate power flow among input sources and the load. Three different power operation modes are defined for the converter and its corresponding transfer function matrix is obtained in each operation mode.

In addition, the designed converter closed-loop control system is highly stable for the all possible operating points. The simulation results are verified by a low power range laboratory prototype with an acceptable efficiency. The proposed converter has the merits of making use of low-voltage batteries, working in stable margin operating points in addition to the advantages of bidirectional power flow at the storage port, simple structure.

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HYBRID WIND-SOLAR ENERGY

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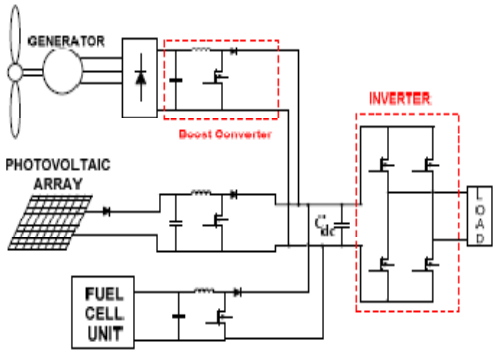
Abstract:- The Main Objective Of A Hybrid-Wind Solar Enegy System Is To Present A New System Configuration Of The Front-End Rectifier Stage For A Hybrid Wind/Photovoltaic Energy System. This Configuration Allows The Two Sources To Supply The Load Separately Or Simultaneously Depending On The Availability Of The Energy Sources. The Characteristic Nature Of This Cuk-Sepic Fused Converter, Additional Input Filters Are Not Necessary To Filter Out High Frequency Harmonics. Harmonic Content Determines The Generator Lifetime, Heating Issues, And Efficiency. The Fused Multi Input Rectifier Stage Allows Maximum Power Point Tracking (Mppt) To Extract Maximum Power From The Wind And Sun When It Is Available. A Suitable Mppt Process Will Be Used For The Wind System And A Standard Disturbance Which Observes The Method Used For The Pv System.The Major Application Of This Project Is It Can Be Used In Distributed Generation Application And Also In Constant & Variable Speed Wind Energy Conversion System And Photovoltaic Energy System. The Technique For Electrical Power System A Hybrid Wind Turbine And Solar Cell System Are Implemented With Goal Such As To Be Completely Different From Traditional Electricity Lab.This Traditional Hybrid Power System Is Too Expensive And Labour Intensive For Industrial Technology Departments Therefore Many Benefits Are Extracted By Using This New System Such As Pv Panel, Batteries And Inverter, Dc Motor. It Is Used In The Production Of Wind Power, Solar Power, Geothermal And Hydroelectric Power Etc.

INTRODUCTION

Since Finite Fossil Fuels On The Earth Have Been Continue Consumed For Several Hundreds Of Years And They Have Been Rapidly Decreased In Recent Years, So We Realize The Importance Of Renewable Energy Development, And Utilization Of Such Important Energy [1-2]. Wind Energy With High-Power Density Is An Important Renewable Energy Having Highly Cost Effective Characteristics. Wind And Photovoltaic Energy Holds The Most Potential To Meet Our Energy Demands. Alone, Wind Energy Is Capable Of Supplying Large Amounts Of Power But Its Presence Is Highly Unpredictable As It Can Be Here One Moment And Gone In Another. Similarly, Solar Energy Is Present Throughout The Day But The Solar Irradiation Levels Vary Due To Sun Intensity And Unpredictable Shadows Cast By Clouds, Birds, Trees, Etc The Common Inherent Drawback Of Wind And Photovoltaic Systems Are Their Intermittent Natures That Make Them Unreliable. However, By Combining These Two Intermittent Sources And By Incorporating Maximum Power Point Tracking (Mppt) Algorithms, The System's Power Transfer Efficiency And Reliability Can Be Improved Significantly.

In This Paper We Are Using An Alternative Multi Input Source Is Used For Hybrid Wind-Solar Energy System. This Desiegn Contain A Combination Of Cuk And Speic Converter. The Feature Of Proposed Topology Are :- 1) The Inherent Nature Of These Two Converter Eliminates The Need Of Separate Input Filter. 2) It Can Be Used For Both Step Up And Step Down Operation (Can Support Wide Range Of Pv And Wind Input). 3) Maximum Power Point Tracking Can Be Realised For Each Source. 4) Single And Dynamic Operation Can Be Performed.

Representation Of Hybrid Wind-Solar Energ



II. PROPOSED MULTI-INPUT RECTIFIER STAGE

A System Diagram Of The Proposed Rectifier Stage Of A Hybrid Energy System Is Shown In Figure 2, Where One Of The Inputs Is Connected To The Output Of The Pv Array And The OtherInput Connected To The Output Of A Generator. The Fusion Of TheTwo Converters Is Achieved By Reconfiguring The Two Existing Diodes From Each Converter And The Shared Utilization Of The Cuk Output Inductor By The Sepic Converter. This Configuration Allows Each Converter To Operate Normally Individually In The Event That One Source Is Unavailable. Figure 3 Illustrates The Case When Only The Wind Source Is Available.In This Case, D1 Turns Off And D2 Turns On; The Proposed Circuit Becomes A Sepic Converter And The Input To Output Voltage Relationship Is Given By (1). On The Other Hand, If Only The Pv Source Is Available, Then D2 Turns Off And D1 Will Always Be On And The Circuit Becomes A Cuk Converter As Shown In Figure 4. The Input To Output Voltage Relationship

Is Given By (2). In Both Cases, Both Converters Have Step-Up/Down Capability, Which Provide More Design Flexibility In The System If Duty Ratio Control Is Utilized To Perform Mppt Control.

$$\frac{V_{dc}}{V_W} = \frac{d_2}{1-d_2} \quad (1)$$

$$\frac{V_{dc}}{V_{PV}} = \frac{d_1}{1-d_1} \quad (2)$$

Figure 5 Illustrates The Various Switching States Of The Proposed Converter. If The Turn On Duration Of M1 Is Longer Than M2, Then The Switching States Will Be State I, Ii, Iv. Similarly, The Switching States Will Be State I, Iii, Iv If The Switch Conduction Periods Are Vice Versa. To Provide A Better Explanation, The Inductor Current Waveforms Of Each Switching State Are Given As Follows Assuming That D2 > D1; Hence Only States 1,2,3 Are Discussed In This Example. In The Following, Ii,Pv Is The Average Input Current From The Pv Source; Ii,W Is The Rms Input Current After The Rectifier (Wind Case); And Idc Is The Average System Output Current. The Key Waveforms That Illustrate The Switching States In This Example Are Shown In Figure 6. The Mathematical Expression That Relates The Total Output Voltage And The Two Input Sources Will Be Illustrated In The Next Section.

State1 (M1 And M2 On)

$$i_{L1} = I_{i,PV} + \frac{V_{PV}}{L_1}t \qquad 0 < t < d_1 T_s$$

$$i_{L2} = I_{dc} + \left(\frac{v_{c1} + v_{c2}}{L_2}\right)t \qquad 0 < t < d_1 T_s$$

$$i_{L3} = I_{i,W} + \frac{V_W}{L_3}t \qquad 0 < t < d_1 T_s$$

State 2 (M1 Off M2on)

$$i_{L1} = I_{i,PV} + \left(\frac{V_{PV} - v_{c1}}{L_1}\right)t \qquad d_1 T_s < t < d_2 T_s$$

$$i_{L2} = I_{dc} + \frac{v_{c2}}{L_2}t \qquad d_1 T_s < t < d_2 T_s$$

$$i_{L3} = I_{i,W} + \frac{V_W}{L_3}t \qquad d_1 T_s < t < d_2 T_s$$

State Iv (M1 Off, M2 Off):

$$i_{L1} = I_{i,PV} + \left(\frac{V_{PV} - v_{c1}}{L_1}\right)t \qquad d_2 T_s < t < T_s$$

$$i_{L2} = I_{dc} \quad \frac{V_{dc}}{L_2}t \qquad d_2 T_s < t < T_s$$

$$i_{L3} = I_{i,W} + \left(\frac{V_W - v_{c1} - V_{dc}}{L_3}\right)t \qquad d_2 T_s < t < T_s$$

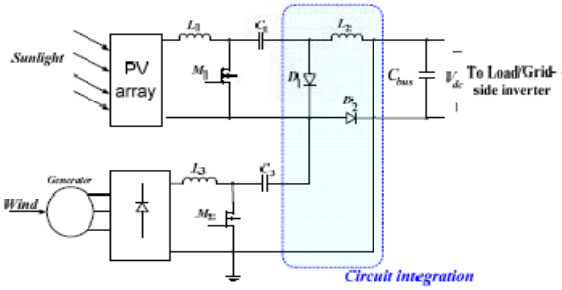


Figure 2: Proposed Rectifier Stage For A Hybrid Wind/Pv System

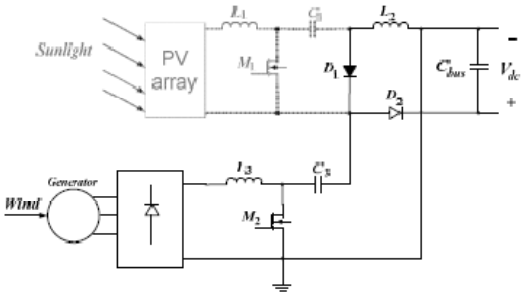


Figure 3: Only Wind Source Is Operational (Sepic)

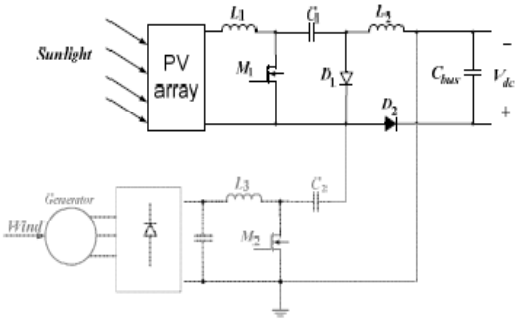
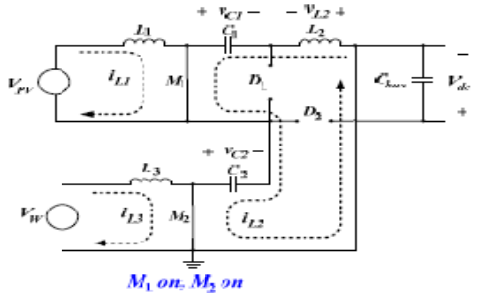


Figure 4: Only Pv Source Is Operation (Cuk)



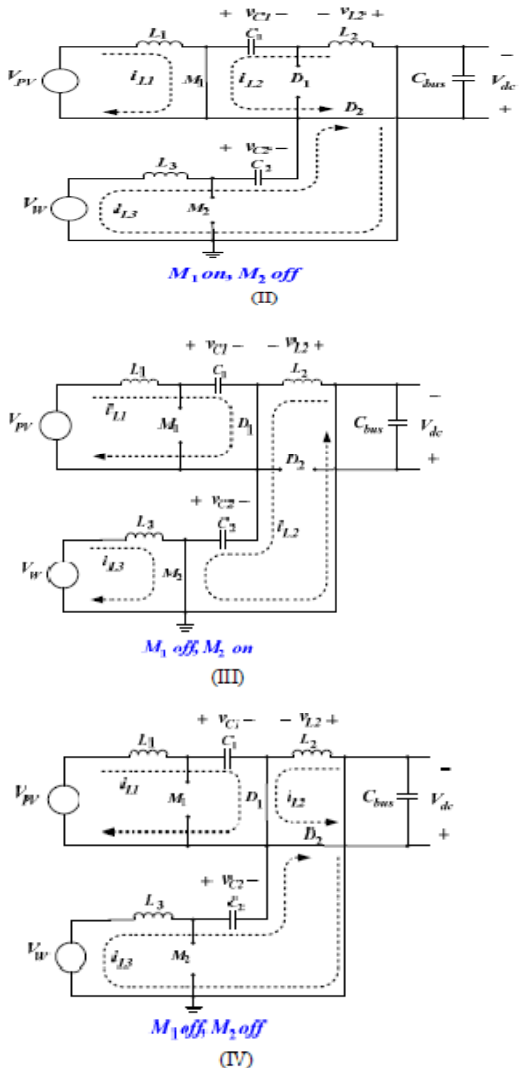


Figure 5 (I-Iv): Switching States Within A Switching Cycle

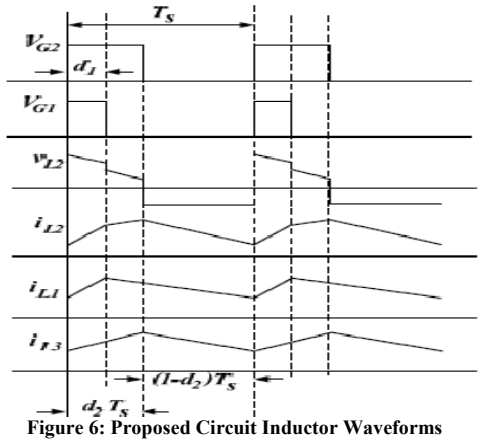


Figure 6: Proposed Circuit Inductor Waveforms

Find An Expression For The Output Dc Bus Voltage, Vdc, The Volt-Balance Of The Output Inductor, L2, Is Examined According To Figure 6 With D2 > D1. Since The Net Change In The Voltage Of L2 Is Zero, Applying Volt-Balance To L2 Results In (3). The Expression That Relates The Average Output Dc Voltage (Vdc) To The Capacitor Voltages (Vc1 And Vc2) Is Then

$$(v_{c1}+v_{c2})d_1T_s+(v_{c2})(d_2-d_1)T_s+(1-d_2)(-V_{dc})T_s=0 \quad (3)$$

$$V_{dc}=\left(\frac{d_1}{1-d_2}\right)v_{c1}+\left(\frac{d_2}{1-d_2}\right)v_{c2} \quad (4)$$

$$V_{dc}=\left(\frac{d_1}{1-d_1}\right)V_{PV}+\left(\frac{d_2}{1-d_2}\right)V_w \quad (5)$$

Obtained As Shown In (4), Where Vc1 And Vc2 Can Then Be Obtained By Applying Volt-Balance To L1 And L3 [9]. The Final Expression That Relates The Average Output Voltage And The Two Input Sources (Vw And Vpv) Is Then Given By (5). It Is Observed That Vdc Is Simply The Sum Of The Two Output Voltages Of The Cuk And Sepic Converter. This Further Implies That Vdc Can Be Controlled By D1 And D2 Individually Or Simultaneously.

The Switches Voltage And Current Characteristics Are Also Provided In This Section. The Voltage Stress Is Given By (6) And (7) Respectively. As For The Current Stress, It Is Observed From Figure 6 That The Peak Current Always Occurs At The End Of The On-Time Of The Mosfet. Both The Cuk And Sepic Mosfet Current Consists Of Both The Input Current And The Capacitors (C1 Or C2) Current. The Peak Current Stress Of M1 And M2 Are Given By (8) And (10) Respectively. Leq1 And Leq2, Given By (9) And (11), Represent The Equivalent Inductance Of Cuk And Sepic Converter Respectively. The Pv Output Current, Which Is Also Equal To The Average Input Current Of The Cuk Converter Is Given In (12). It Can Be Observed That The Average Inductor Current Is A Function Of Its Respective Duty Cycle (D1). Therefore By Adjusting The Respective Duty Cycles For Each Energy Source, Maximum Power Point Tracking Can Be Achieved.

$$v_{ds1}=V_{pv}\left(1+\frac{d_1}{1-d_1}\right) \quad (6)$$

$$v_{ds2}=V_w\left(1+\frac{d_2}{1-d_1}\right) \quad (7)$$

$$i_{ds1,pk}=I_{i,PV}+I_{dc,avg}+\frac{V_{PV}d_1T_s}{2L_{eq1}} \quad (8)$$

$$L_{eq1}=\frac{L_1L_2}{L_1+L_2} \quad (9)$$

$$i_{ds2,pk}=I_{i,W}+I_{dc,avg}+\frac{V_W d_2T_s}{2L_{eq2}} \quad (10)$$

$$L_{eq2}=\frac{L_3L_2}{L_3+L_2} \quad (11)$$

$$I_{i,PV}=\frac{P_o}{V_{dc}}\frac{d_1}{1-d_1} \quad (12)$$

Mppt Control Of Proposed Circuit A Common Inherent Drawback Of Wind And Pv Systems Is The Intermittent Nature Of Their Energy Sources. Wind Energy Is Capable Of Supplying Large Amounts Of Power But Its Presence Is Highly Unpredictable As It Can Be Here One Moment And Gone In Another. Solar Energy Is Present Throughout The Day, But The Solar Irradiation Levels Vary Due To Sun Intensity And Unpredictable Shadows Cast By Clouds, Birds, Trees, Etc. These Drawbacks Tend To Make These Renewable Systems Inefficient. However, By Incorporating Maximum Power Point Tracking (Mppt) Algorithms, The Systems' Power Transfer Efficiency Can Be Improved Significantly. To Describe A Wind Turbine's Power Characteristic, Equation (13) Describes The Mechanical Power That Is Generated By The Wind [6].

$$p_m = 0.5\rho A C_p(\lambda, \beta) v_w^3 \qquad (13)$$

Where
ρ = *air density,*
A = *rotor swept area,*
$C_p(\lambda, \beta)$ = *power coefficient function*
λ = *tip speed ratio,*
β = *pitch angle,*
v_w = *wind speed*

The Power Coefficient (Cp) Is A Nonlinear Function That Represents The Efficiency Of The Wind Turbine To Convert Wind Energy Into Mechanical Energy. It Is Dependent On Two Variables, The Tip Speed Ratio (Tsr) And The Pitch Angle. The Tsr, Λ, Refers To A Ratio Of The Turbine Angular Speed Over The Wind Speed. The Mathematical Representation Of The Tsr Is Given By (14) [10]. The Pitch Angle, B, Refers To The Angle In Which The Turbine Blades Are Aligned With Respect To Its Longitudinal Axis.

$$\lambda = \frac{R\,\omega_b}{v_w} \qquad (14)$$

Where
R = *turbine radius,*
ω_b = *angular rotational speed*

Figure 7 And 8 Are Illustrations Of A Power Coefficient Curve And Power Curve For A Typical Fixed Pitch (B =0) Horizontal Axis Wind Turbine. It Can Be Seen From Figure 7 And 8 That The Power Curves For Each Wind Speed Has A Shape Similar To That Of The Power Coefficient Curve. Because The Tsr Is A Ratio Between The Turbine Rotational Speed And The Wind Speed, It Follows That Each Wind Speed Would Have A Different Corresponding Optimal Rotational Speed That Gives The Optimal Tsr. For Each Turbine There Is An Optimal Tsr Value That Corresponds To A Maximum Value Of The Power Coefficient (Cp,Max) And Therefore The Maximum Power. Therefore By Controlling Rotational Speed, (By Means Of Adjusting Theelectrical Loading Of The Turbine Generator) Maximum Power Can Be Obtained For Different Wind Speeds.

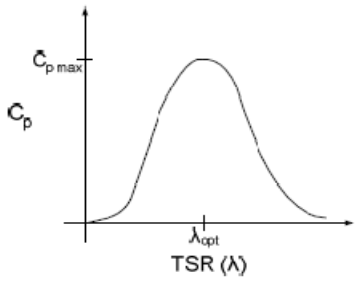


Figure 7: Power Coefficient Curve For A Typical Wind Turbine

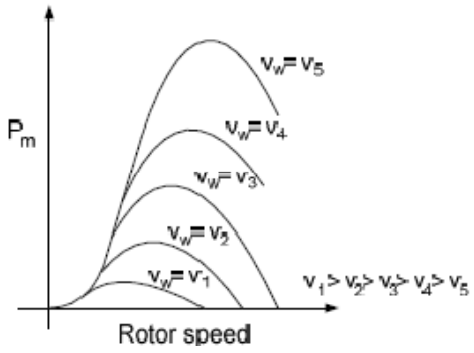


Figure 8: Power Curves For A Typical Wind Turbine A Solar Cell Is Comprised Of A P-N Junction Semiconductor

That Produces Currents Via The Photovoltaic Effect. Pv Arrays Are Constructed By Placing Numerous Solar Cells Connected In Series And In Parallel [5]. A Pv Cell Is A Diode Of A Large-Area Forward Bias With A Photovoltage And The Equivalent Circuit Is Shown By Figure 9 [11]. The Current-Voltage Characteristic Of A Solar Cell Is Derived In [12] And [13] As Follows:

$$I = I_{ph} - I_D \qquad (15)$$

$$I = I_{ph} - I_0\left[\exp\left(\frac{q(V + R_s I)}{Ak_B T}\right) - 1\right] - \frac{V + R_s I}{R_{sh}} \qquad (16)$$

Where

Iph = Photocurrent,

Id = Diode Current,

I0 = Saturation Current,

A = Ideality Factor,

Q = Electronic Charge 1.6x10-9,

Kb = Boltzmann's Gas Constant (1.38x10-23),

T = Cell Temperature,

Rs = Series Resistance,

Rsh = Shunt Resistance,

I = Cell Current,

V = Cell Voltage

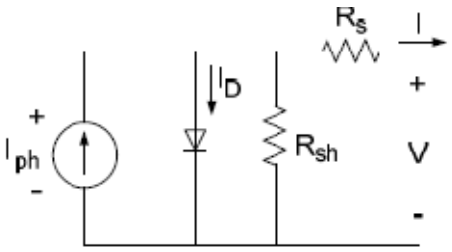
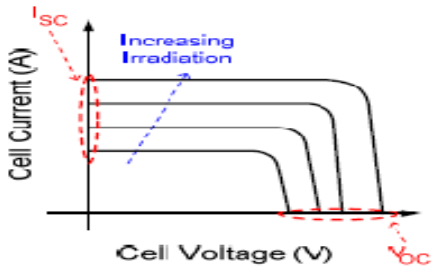


Figure 9: Pv Cell Equivalent Circuit

Typically, The Shunt Resistance (Rsh) Is Very Large And The Series Resistance (Rs) Is Very Small [5]. Therefore, It Is Common To Neglect These Resistances In Order To Simplify The Solar Cell Model. The Resultant Ideal Voltage-Current Characteristic Of A Photovoltaic Cell Is Given By (17) And Illustrated By Figure 10. [5]

$$I = I_{ph} - I_0\left(\exp\left(\frac{qV}{kT}\right) - 1\right) \qquad (17)$$



The Typical Output Power Characteristics Of A Pv Array Under Various Degrees Of Irradiation Is Illustrated By Figure 11. Itcan Be Observed In Figure 11 That There Is A Particular Optimal Voltage For Each Irradiation Level That Corresponds To Maximum Output Power. Therefore By Adjusting The Output Current (Or Voltage) Of The Pv Array, Maximum Power From The Array Can Be Drawn.

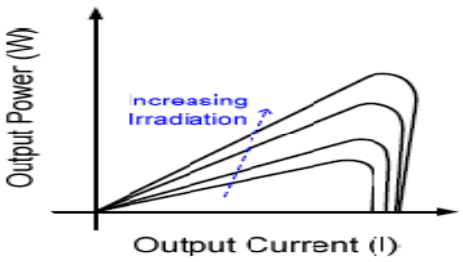


Figure 11: Pv Cell Power Characteristics

Due To The Similarities Of The Shape Of The Wind And Pv Array Power Curves, A Similar Maximum Power Point Tracking Scheme Known As The Hill Climb Search (Hcs) Strategy Is Often Applied To These Energy Sources To Extract Maximum Power. The Hcs Strategy Perturbs The Operating Point Of The System And Observes The Output. If The Direction Of The Perturbation (E.G An Increase Or Decrease In The Output Voltage Of A Pv Array) Results In A Positive Change In The Output Power, Then The Control Algorithm Will Continue In The Direction Of The Previous Perturbation. Conversely, If A Negative Change In The Output Power Is Observed, Then The Control Algorithm Will Reverse The Direction Of The Pervious Perturbation Step. In The Case That The Change In Power Is Close To Zero (Within A Specified Range) Then The Algorithm Will Invoke No Changes To The System Operating Point Since It Corresponds To The Maximum Power Point (The Peak Of The Power Curves).

The Mppt Scheme Employed In This Paper Is A Version Of The Hcs Strategy. Figure 12 Is The Flow Chart That Illustrates The Implemented Mppt Scheme.

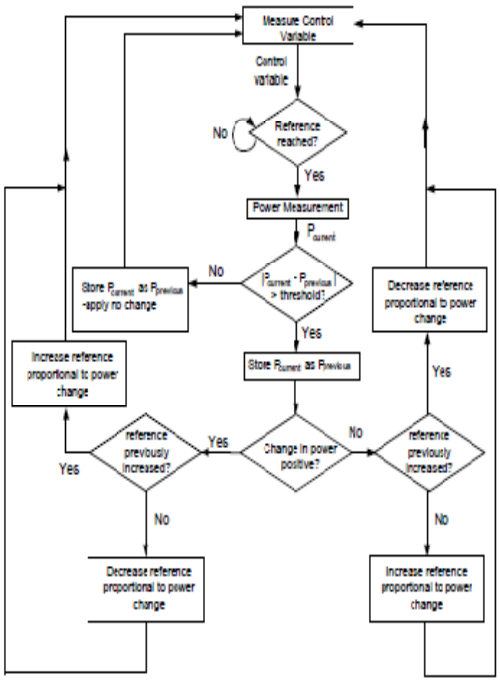


Figure 12: General Mppt Flow Chart For Wind And Pv

Driver Circuit:

It Is Used To Provide 9 To 20 Volts To Switch The Mosfet Switches Of The Inverter. Driver Amplifies The Voltage From Microcontroller Which Is 5volts. Also It Has An Optocoupler For Isolating Purpose . So Damage To Mosfet Is

Prevented.

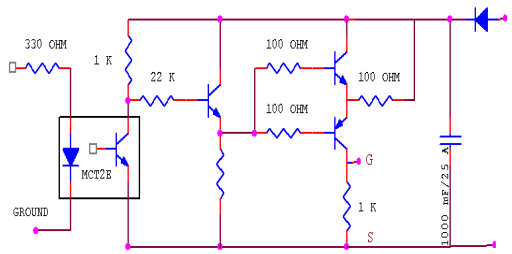


Fig 2.5:Driver Circuit.

Driver Circuit Operation:

The Driver Circuit Forms The Most Important Part Of The Hardware Unit Because It Acts As The Backbone Of The Inverter Because It Gives The Triggering Pulse To The Switches In The Proper Sequence. The Diagram Given Above Gives The Circuit Operation Of The Driver Unit. The Driver Unit Contains The Following Important Units.

Optocoupler

Totem Pole

Capacitor Supply

Diode

Resistor

2.13. Optocoupler:

Optocoupler Is Also Termed As Optoisolator. Optoisolator A Device Which Contains A Optical Emitter, Such As An Led, Neon Bulb, Or Incandescent Bulb, And An Optical Receiving Element, Such As A Resistor That Changes Resistance With Variations In Light Intensity, Or A Transistor, Diode, Or Other Device That Conducts Differently When In The Presence Of Light. These Devices Are Used To Isolate The Control Voltage From The Controlled Circu

3.2. Features Of Pic Microcontroller :

The Microcontroller Has The Following Features:

1.High-Performance Risc Cpu:

• Only 35 Single- Word Instructions To Learn .Hence It Is User Friendly.Easy To Use

• All Single - Cycle Instructions Except For Program Branches, Which Are Two-Cycle

• Operating Speed: Dc – 20 Mhz Clock Input Dc – 200 Ns Instruction Cycle

• Up To 8k X 14 Words Of Flash Program Memory, Up To 368 X 8 Bytes Of Data Memory(Ram), Up To 256 X 8 Bytes Of Eeprom Data Memory. It Is Huge One

2.Peripheral Features:

• Timer0: 8-Bit Timer/Counter With 8 – Bit Prescaler. It Is Used For Synchronisation

• Timer1: 16-Bit Timer/Counter With Prescaler, Can Be Incremented During Sleep

• Timer2:8-Bit Timer/Counter With 8-Bit Period Register, Prescaler And Postscaler

• Two Capture , Compare And Some Pwm Modules, Having Following Features

- Capture Is 16-Bit, Max. Resolution Is 12.5 Ns

- Compare Is 16-Bit, Max . Resolution Is 200 Ns

- Pwm Maximum Resolution That Is 10-Bit

Synchronous Serial Port (Ssp) With Spi (Master Mode) And I^2c(Master/Slave)

Universal Synchronous Asynchronous Receiver Transmitter With 9 Bit Address

Parallel Slave Port (Psp) 8 Bits Wide With External Rd, Wr And Cs Controls

3.Analog Features:

It Has An Analog Comparator Module With:

(1)Two Analog Comparators

(2) Programmable On-Chip Voltage Reference (Vref) Module (3)Programmable Input Multiplexing From Device Inputs And Internal Voltage Reference Thus 3 Parts

4.Cmos Tech

It Has Following Features:

(1)Low-Power, High-Speed Flash/Eeprom Technology

(2)Fully Static Design

(3)Wide Operating Voltage Range (2.0v To 5.5v)

(4) Commercial And Industrial Temperature Ranges

(5)Low-Power Consumption

Fig 3.3: Triggering Circuit.

Simulation Results

In This Section, Simulation Results From Psim 8.0.7 Is Given To Verify That Proposed Multi-Input Rectifier Stage Can Support Individual As Well As Simultaneous Operation. Thespecifications For The Design Example Are Given In Table I. Figure 13 Illustrates The System Under The Condition Where The Wind Source Has Failed And Only The Pv Source (Cuk Converter Mode) Is Supplying Power To The Load. Figure 14 Illustrates The System Where Only The Wind Turbine Generates Power To The Load (Sepic Converter Mode). Finally, Figure 15 Illustrates The Simultaneous Operation (Cuk-Sepic Fusion Mode) Of The Two Sources Where M2 Has A Longer Conduction Cycle (Converter States I, Iv And Iii—See Figure 5).

Table I. Design Specifications

Output power (W)	3kW
Output voltage	500V
Switching frequency	20kHz

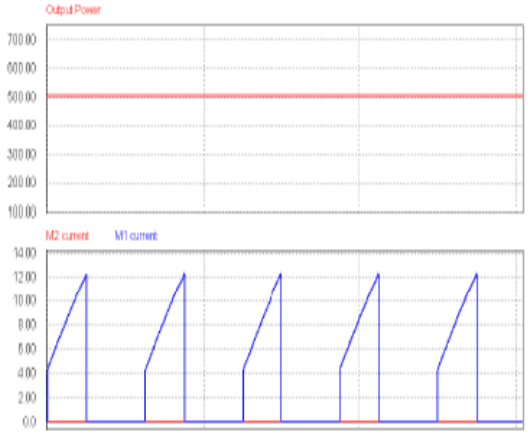
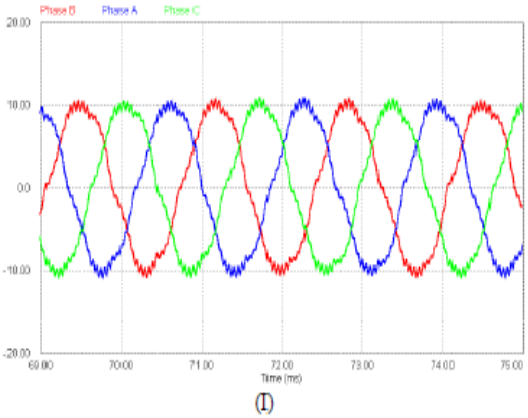


Figure 13 : Individual Operation With Only Pv Source (Cuk Operation) Top: Output Power, Bottom: Switch Currents(M1andM2)



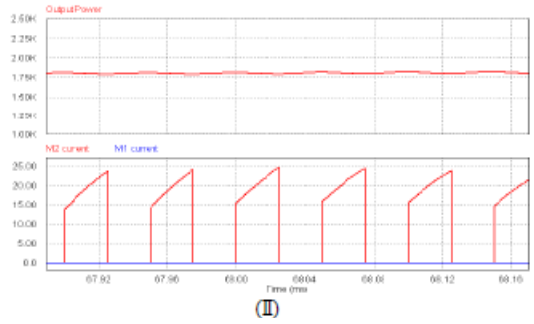


Figure 14 : Individual Operation With Only Wind Source (Sepic Operation) (I) The Injected Three Phase Generator Current; (Ii) Top: Output Power, Bottom: Switch Currents (M1 And M2)

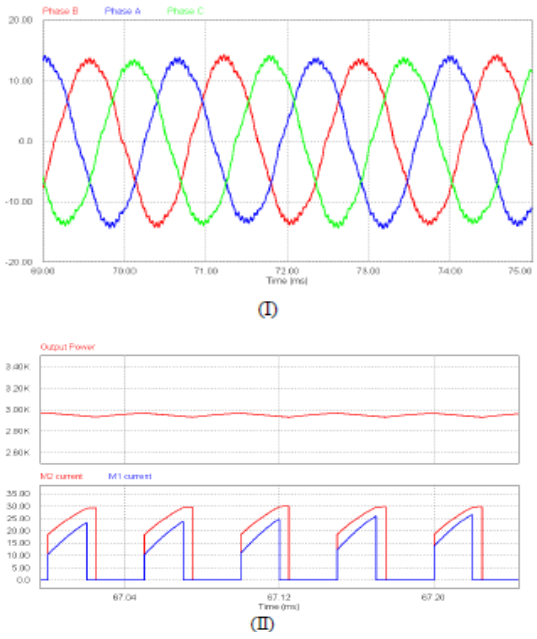


Figure 15 : Simultaneous Operation With Both Wind And Pv Source (Fusion Mode With Cuk And Sepic)(I) The Injected Three Phase Generator Current; (Ii) Top: Output Power, Bottom: Switch Currents (M1 And M2)

Figure 16 And 17 Illustrates The Mppt Operation Of The Pv Component Of The System (Cuk Operation) And The Wind Component Of The System (Sepic Operation) Respectively.

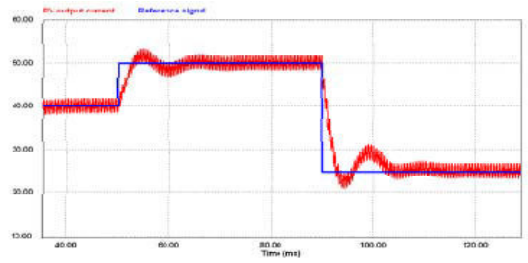


Figure 16 : Solar Mppt – Pv Output Current And Reference Current Signal (Cuk Operation)

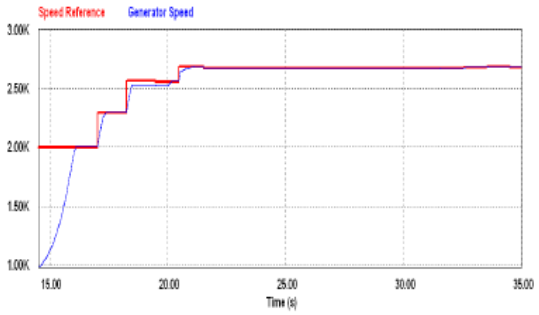


Figure 17 : Wind Mppt – Generator Speed And Reference Speed Signal (Sepic Operation)

CONCLUSION

In This Paper A New Multi-Input Cuk-Sepic Rectifier Stage For Hybrid Wind/Solar Energy Systems Has Been Presented. The Features Of This Circuit Are: 1) Additional Input Filters Are Not Necessary To Filter Out High Frequency Harmonics; 2) Both Renewable Sources Can Be Stepped Up/Down (Supports Wideranges Of Pv And Wind Input); 3) Mppt Can Be Realized For Each Source; 4) Individual And Simultaneous Operation Is Supported. Simulation Results Have Been Presented To Verify The Features Of The Proposed Topology.

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VISION OF SMART SUSTAINABLE HOME & HOME APPLICATION MADE REAL, USING LABVIEW

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Abstract— Each of us needs comfort and safety in our life. Many real systems used in building don't have the flexibility and the ability to give users all comfort and safety that they need. Making a complete system is a big challenge because of the need to make many controlling system which can run in the same time. So, the main objective of this project is to provide fully automatic, secured and energy efficient home and home applications and controlling features. Our project include many system which controlled by lab view such as:- Fire alarm system ,burglary alarm system, internal light system, external light system, remote control system, conditioning system, power supplies switching system and garage door system.

Keywords— *Multiple monitoring and control, lab view application, automatic cleaning robot, automatic irrigation technique, automatic secured, energy efficient.*

I. INTRODUCTION

Making a complete system is a big challenge because of the need to make many controlling system which can run at the same time. Our project include many system which controlled by LabView such as:-

Fire-alarm system,

Burglary alarm system,

Internal light system,

External light system,

Remote control system,

Power supplies switching system,

Garage door system.

The term Building automation refers to an intelligent network of programmable controllers and software that monitors and controls mechanical heating, ventilation and air conditioning equipment, and indoor and outdoor lighting in a building. The primary function of a building automation system or energy management system is to increase the efficiency of a building and reduces energy and maintenance costs. Building Automation systems optimize the performance and maintenance of multiple building control systems including; •Heating, ventilation, and air conditioning (HVAC) – These systems include central plants, air handling units, package units and fan coils. •Lighting systems – including indoor and outdoor systems. •Metering systems – including electrical meters, gas meters and BTU meters. There are two major components to building automation systems; the user interface software and the controller. The user interface is typically a computer based graphical software application that allows the user to interface with the system and provides the user full control over the building automation system. A controller is an electronic device that monitors and changes the operations of a specific system. The operational conditions include output variables of the system which can be affected by adjusting certain inputs. The communication between these two components is achieved through special and dedicated network resources. In this paper we decide to take a different approach. The buildings which are used as offices for companies, hospitals, universities, schools, etc…, have installed their computer network to carry data for their own businesses. Also, almost every room in these buildings has at least one PC connected to the buildings Local Area Network (LAN). These network resources can be used as the infrastructure for the building automation system as well.

II. SYSTEM DESCRIPTION

A. Basic Principle:-

Our system works on logical analysis. In detailed, the LabView application taking various input from connected sensors and processes it according to defined program and then it provides logical output to whole house's power system. Its additional features is that it having power protection system also, so when any fault occurs inside home the protection system immediately traps the main power source.

B.CONSTRUCTION

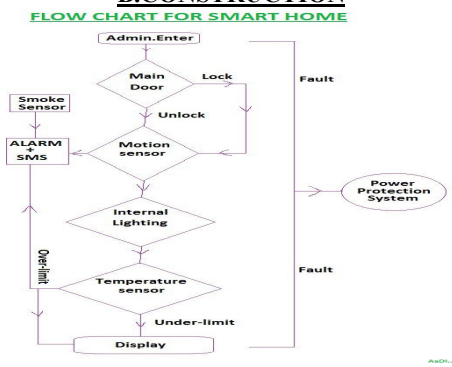

Fig.1

(i) EXTERNAL LIGHTING :-

Lighting system depends on a **sun cell** reading that and give it to LabVIEW software to analysts it. So LabVIEW software has an indicator about day and night time of in order to control the status of external light lamps.

It will be used to switching ON & OFF automatically for garden light, balcony light etc.

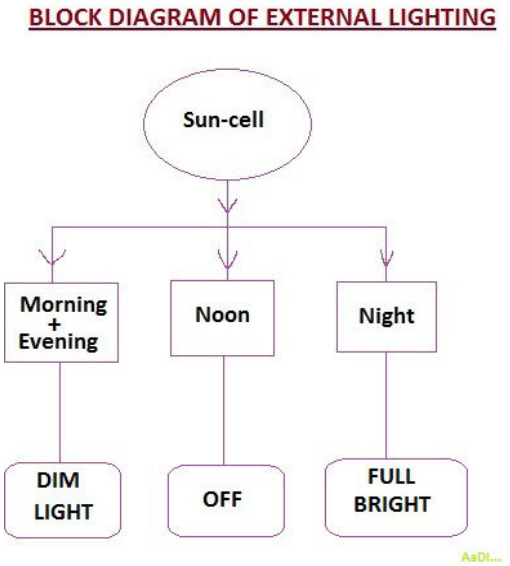

Fig.2

(ii) Internal Lighting:-

The internal lighting system consists of a PIR-motion sensor, dimmer and lamps which have a direct control by LabView software. This system will make an automatically lighting in the house when there is any movement inside it.

The additional feature is that the user can change the brightness of light according to his mood.

(iii) Fire Alarm System & Burglar Alarm System:-

When an fire (or Burglary) happen in house, LabView will receive signal from fire (or burglary) sensors , and can be able to send SMS to two different mobiles and run the fire alarm siren as user need.

(iv) Temperature System:-

The basic thing in temperature system is the reading of temperature value from temperature sensor.
For that, we are using LM35 temperature sensor. LabVIEW read the signal from LM35 sensor as variable analog value.
After processing the value it will be displayed to running LabView application.
If at processing time the application reads temperature's value more than maximum limit, it immediately runs the fire alarm and also sends information to admin. & fire station.

(V.) Central Unit and Rooms Unit Remote Control:-

The remote control is used to make some operation in the system by connection it's with LabVIEW software. In addition, it used to control and switching the load in every room in the house using the rooms units receiver in every room.
As well as used alone transmitter remote to control the Garage door.

(Vi.) Application Features:-

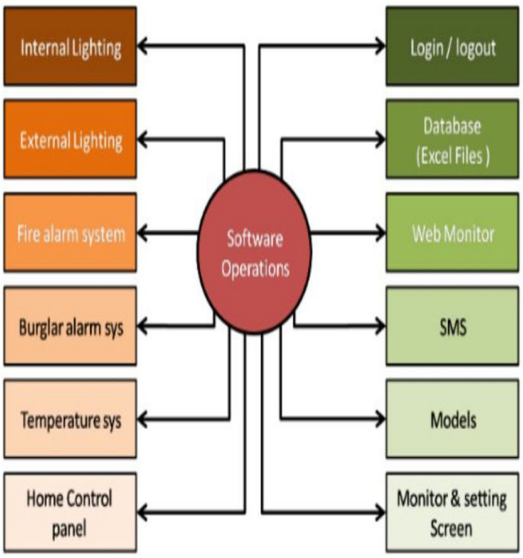

Fig.3

C. Home Application

a) Automatic Cleaning Robot:-

The name itself tells all about it as, it is fully automatic robot which can be used for cleaning purpose in any environment i.e. dry or wet surface.
It having inbuilt vacuum that sucks all small particle & garbage and then wiper cleans the surface.

b) Automatic Irrigation Technique:-

This technique we are using for gardening.
Where the humidity sensor will sense the amount of humid present in soil and then it will send signal to motor to turn ON or OFF through microcontroller.

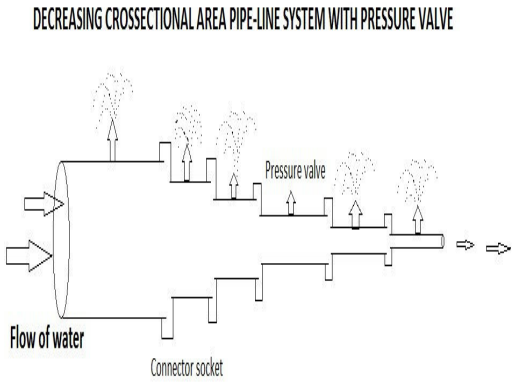

Fig.4

Advanced Pipe Line System:-

We connected pressure valve at different positions of our pipe-line as crop distance for equal water distribution. It is well known that, when water will go forward its pressure and velocity will be decreased, so we gradually decrease the crossectional area of pipe-line with increasing length of distribution. Due to this, pressure & velocity will be maintained at last end of the pipe-line.

III.LABVIEW PROGRAM

EXTERNAL LIGHTING :-

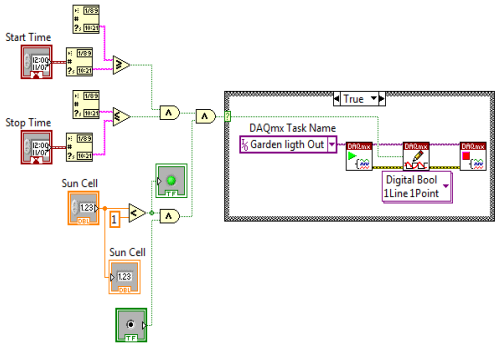

FIG.5

INTERNAL LIGHTING:-

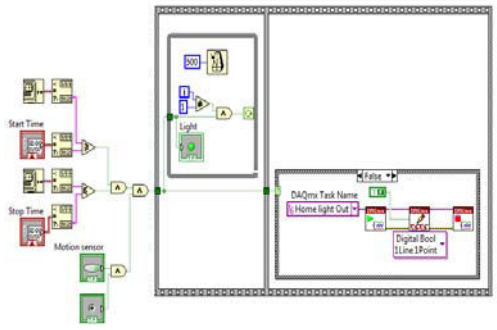

Fig.6

Fire Alarm System & Burglar Alarm System:-

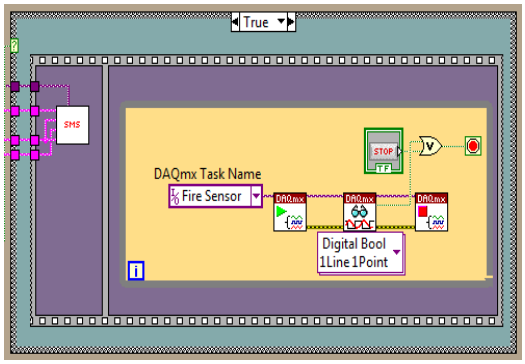

Fig.7

Temperature System:-

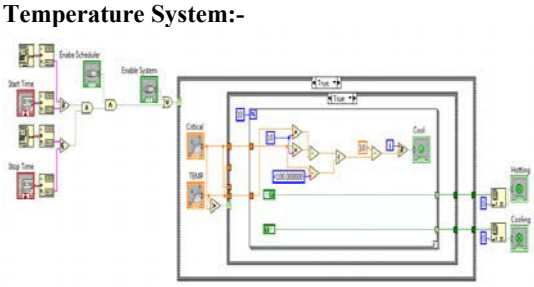

Fig.8

Central Unit and Rooms Unit Remote Control:-

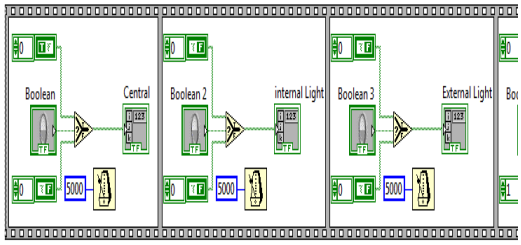

FIG.9

IV. CONCLUSIONS

Smart home technology is becoming increasingly more common to ordinary consumers, and the owner of many new building projects are proud to announce it, if the flats are fitted with "new, intelligent technology". There is a responsibility resting on governmental bodies and professionals to involve in the future planning of community care, to ensure that technology are used to assist the human helpers that always will be the basis in all care.

- ✓ The LabView based application is user friendly application, which we developed.
- ✓ No need of any other additional home management system.
- ✓ The system is fully secured and it keeps home environment secured also.
- ✓ In multiple way user can monitor and control.

- ✓ It is fully automatic, secured and energy efficient formula.
- ✓ The additional feature of home application makes the whole system more efficient.

ACKNOWLEDGMENT

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REVIEW ON AUTOMATION AND BIDIRECTIONAL DATA TRANSFER BASED ON PLCC

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Abstract–This paper proposes a new effective communication using PLCC(power line carrier communication) techniques. The controlling, monitoring and protection of smart grid, AMR(automatic meter reading) ,home appliance energy monitoring, energy controlling and noise reduction scheme of smart grid using PLCC is explained briefly. Some communication protocol, basic architecture of plcc and better performance is analysed by software and simulation results is applied on system model.

Keywords: *smart grid, lvdc, AMR, plc, noise reduction, Railway control*

I INTRODUCTION

Over the past few years, the electric power industry, state and federal regulators, government agencies, and universities have been considering with how to best update the aging electric power infrastructure. The required infrastructure for the smart grid including measurement and communication requirements is presented in this paper. From these considerations, The smart grid technology has attracted public attention. The goal of the smart grid is to use advanced, information-based technologies to increase power grid efficiency, reliability, and flexibility and reduce the rate at which additional electric utility infrastructure needs to be built(a),(b). To support the smart grid and meet the customer's desire, communication technologies should be considered fast data rate, reliable reception and access in anywhere. As one of the promising candidates for smart grid, power line carrier communication (PLCC) is a leading technique because of its advantages. the most striking point is the installation cost is very less than other communication system with bidirectional data communication. The structure of these paper is organised as follows. In section II the architecture for LVDC system, PLCC based AMR system is represented in section III, home appliance energy monitoring and controlling is assessed in section IV,PLCC model for electric energy power control is presented in section V, The noise reduction scheme for smart grid is in section VI and performance and simulation results of each section is shown in subdivision of each section. Finally section VII concludes the paper.

II. PLC-BASED NETWORK ARCHITECTURE FOR LVDC DISTRIBUTION SYSTEM

2.1COMMUNICATION REQUIREMENTS IN LVDC SYSTEM

LVDC Smart Grid Concept

The main objectives in developing distribution systems and pursuing for smart grids are cost efficiency and the reliability of the electricity distribution. The LVDC system is designed to replace both traditional medium-voltage (MV) overhead line branches and low-voltage AC distribution with a low-voltage DC distribution system implemented with underground cabling. The structure of the LVDC system with the proposed PLC-based network is illustrated in Fig. a. The medium voltage AC is transformed and rectified to low-voltage DC and distributed to customers. The rectified DC is then smoothed. DC power is delivered to customers with AXMK cables in a proposed bipolar LVDC system .In LVDC system, the maximum allowed low voltage 1500 VDC is achieved with the arrangement of three voltage levels; +750, 0, and –750 VDC. The LVDC system between the rectifier and the customers is constructed with 500-meter long AXMK cables. The ±750 VDC conductors of the underground AXMK cable are coupled to the corresponding conductors at every over ground cable connection cabinet since the grid, while the two N conductors of every AXMK cable end are short-circuited.

Each customer has an inverter, which produces the suitable AC voltage for the customer loads. With the LVDC system, it could be possible in the future to move to DC distribution. In addition, the main advantage of

DC for the smart grid is that no synchronization is required for distributed generation

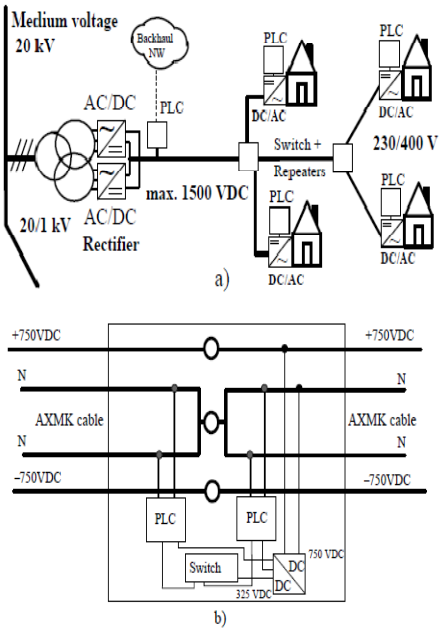


Fig. a) Proposed data transmission concept between customer inverters and a distribution rectifier integrated into the bipolar LVDC system. The rectifier and every customer are equipped with PLC modems including a coupling interface. At the rectifier, there is also a connection to the backhaul network and databases. b) Content of an over ground cable connection cabinet, where the short-circuited N conductor loops and the DC power supply conductors of two AXMK cables are connected to the corresponding conductors. It includes at least two PLC modems and a switch. In addition to the network components, a DC/DC power supply for these components is included.

With the LVDC system, the quality of the AC low voltage supply a the customers can be improved with a customer inverter, and it is possible to shorten and decrease the number of the branches of the MV grid consisting of over headlines by replacing those with underground low-voltage cables. This results directly in a decreased amount of possible faults in the MV grid. Thus, the quality and reliability of the electricity distribution are improved.

2.2 COMMUNICATION ARCHITECTURE FOR LVDC SYSTEM

The structure and dimensions of the propose Communication architecture are mainly defined by the LVDC grid when the communication is implemented with PLC. The LVDC distribution system may cover large area(1-5km). Thus signalling range has to be known . In addition, inverters in the grid generate harmonics and interferences to the channel. These combined with the challenge the implemented functions in the grid set the boundary conditions and the minimum requirements for PLC.

One suitable commercial protocol, Home Plug 1.0, which Provides broadband over power line (BPL) is proposed for Communication method in the grid. Home Plug 1.0 modems operate as bridges across connections in the channel and make it possible to implement an IP-based network with standardized Ethernet packets over the LVDC grid. Thus, the centralizer unit in the proposed network is a commercial router ,which is connected through the Home Plug 1.0modems to every customer in the grid. The router operates as a DHCP (Dynamic Host Configuration Protocol) server, and assigns IP addresses to every customer communication interface Based on the MAC addresses. Hence, an own sub network is formed for every LVDC system.

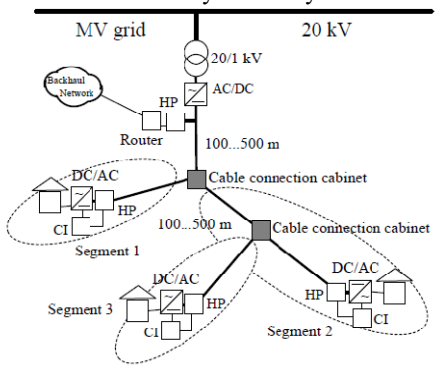


Fig. 4. Basic structure of a PLC-based network divided into data transmission

segments by the Home Plug (HP) modems and Ethernet switches integrated into cable connection cabinets, built into the LVDC grid. Data are transmitted between customers, and a router through the communication channel, which comprises inductive coupling interfaces and AXMK cables.

The communication channel in the LVDC system between the rectifier and the customers is constructed with AXMK cables coupled together according to the structure of the grid. This arrangement makes it possible to divide the communication network into segments (max. 500 m each), when an inductive coupling is formed between the N conductors. According to the structure of the LVDC grid, it is possible that from one cable connection cabinet, there are several AXMK cable outputs to the customers. Hence, every cable connection cabinet is equipped with at least two modems one to communicate up (to the rectifier), and one down (to the inverters).

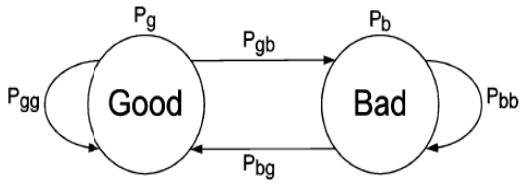
III. PLC BASED AMR SYSTEM

Eeffective communication protocol for the implementation of an automatic meter reading system using power-line communications (PLC) and presents analytical models to study its performance. the “silent node” problem, where a meter unit cannot directly

communicate with the data concentrator (DC) to send and receive data. Communications between the DC and remote devices in the downlink and uplink directions are established through several intermediate relays due to high-level attenuation of power cables. Dynamically creating and managing these multi hop structures efficiently is a main issue in the implementation of AMR systems. The two AMR schemes, clustered simple polling
(CSP) and neighbour relay polling (NRP), introduced in to
overcome the "silent node" problem.

3.1 METER UNIT MODEL

In the two-state Markov model, a meter unit is "Good" which indicates that the particular meter unit can directly communicate with the DC or a relay meter unit and "Bad" which indicates that the meter unit is currently a "silent node." and are the probabilities for a meter unit with "Good" and "Bad" status, respectively



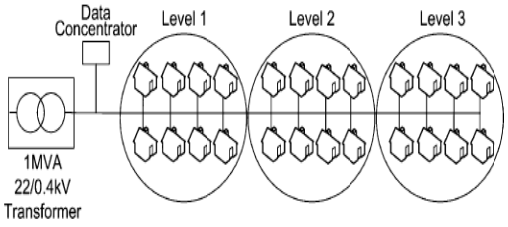
Two-state transition Markov model for a meter unit.

the two-state transition can be represented quantitatively by using (1)–(3), and the local balance concept formulated in (4)

$$P_g + P_b = 1$$
$$P_{gg} + P_{gb} = 1$$
$$P_{bb} + P_{bg} = 1$$
$$P_g P_{gb} = P_b P_{bg}.$$

3.2 PLC ACCESS MODEL

The low-voltage power-supply network is built upon various network topologies, with a tree-like structure .Ideally, all meter units in a sub network communicate directly with the DC to receive and send data, but this communication capability decreases with increasing distance between the meter unit and the DC. The broadcasting method in the proposed protocol will establish a virtual three-level cluster to create a multi hop structure in the PLC access network, as shown in Fig. communication between neighbouring meter units is 100% successful. The neighbour meter unit refers to a meter unit that belongs to the same cluster and phase of the transformer as the "silent node" to ensure minimal signal attenuation during data transmission. The three-level cluster system assumes that the DC can only communicate with "Good" meter units in level 1,but not with meter units in levels 2 and 3.



Access network model.

A PLC access network in an HDB residential area generally consists of about meter units connected through underground cables. The DC is connected to the red, yellow, and blue phases of a three-phase distribution transformer which are subdivided into many sub network .In the three-level cluster system, successful data transmission depends on the relay meter units to transfer data to the next level or to the DC

IV. HOME APPLIANCE ENERGY MONITORING AND CONTROLLING BASED ON POWER LINE COMMUNICATION

4.1. DESIGN OF RMCPS

The circuit diagram of the RMCPS is shown in Fig. 1; it includes the multiple AC power sockets, and a simple plug-in microcontroller which both performs the power on/off of the sockets and processes the measured data.

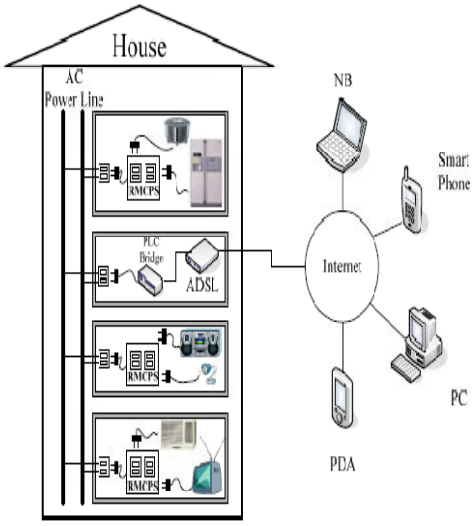


Fig. The RMCPS power supply socket system

The RMCPS also includes a power measuring circuit to measure the power consumption of each electric home appliance. The socket voltage is connected to the MCU through a filter. The socket current then is converted from a current to a voltage. The electrical power comes from multiplying the two voltage

signals with the current signal, and the results are accumulated in the register.

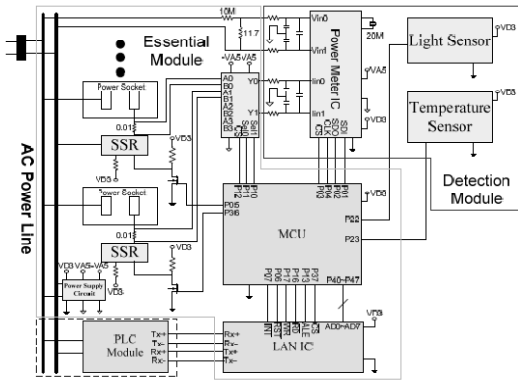


Fig. 2 RMCPS circuit

4.2 SOFTWARE ARCHITECTURE

For the software modules based on a Thin OS core, application programs can be divided into nine parts.

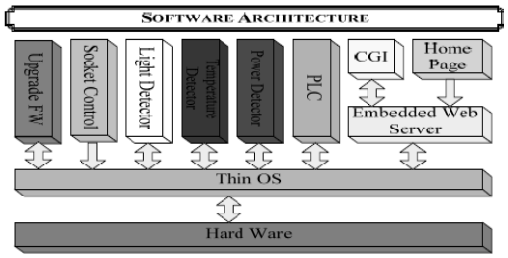


Fig 3 The software structure for remoting monitoring and controlling

Home Page to client application program for remote monitoring and controlling is loaded. By using the spare time available for the embedded Web server, the power consumption, Vrms and Irms of power supply sockets can be read and temporarily saved in memories to wait for Web-page retrieval. After the network packets have been processed by the embedded Web server, if there is a remote user demand, the corresponding process will be connected to CGI applications such as the demands for the Web-page to display a new power socket status, the overall control of the specific on/off operation on power sockets and the firmware (FW) updates. This process convenient for the user to remotely monitor and control the power sockets.

V. PLC MODULE FOR AN ELECTRIC POWER ENERGY MONITORING SYSTEM

PLC is classified into low-speed type and high-speed type. The low-speed PLC is mainly utilized as a home networking system.PLC uses the power lines to be already existed ,the installation of the PLC networks is very easy and low cost. The low-speed PLC module for an electric power energy monitoring system is presented usingST7538Q. This module is applied to rainwater management system to demonstrate its feasibility and effectiveness

5.1 POWER LINE COMMUNICATION MODULE.

A. Rainwater management System

In March 2007, Seoul Metropolitan Government held the Rainwater Management Equipments Exhibition to make a model city of green environment. In this, the amount of rainwater is detected using a water level transmitter. The sensing data is transferred to the main management system. Plc acts as communication method.

B. Power Line Communication Module

ST7538Q manufactured by STMicroelectronics is selected in this paper due to easy of access. It is a half duplex frequency shift keying (FSK) transceiver.

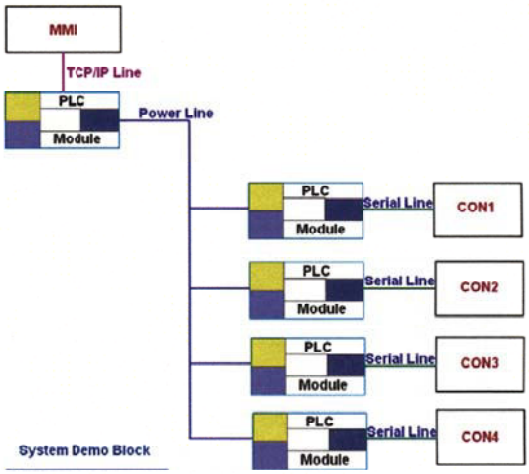
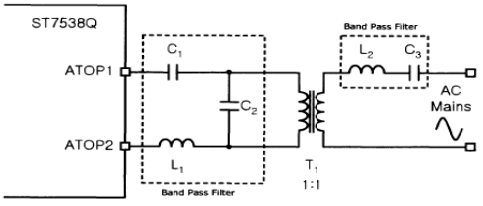


Fig. 4. Total control system structure with PLC modules

The PLC module is installed in each of control unit. The several slave PLC modules are inter faced with a main computer through the power line and the master PLC module. As can be shown in Fig. 4., the total control system applied to an electric power energy monitoring system consists of several PLC modules with the corresponding objects of control. These two parts are connected with a RS-485 serial line. A main PLC module exchanges a command with several slave modules through the power line. Also the main control centre (MMI; Man-Machine Interface) communicates with the main PLC module using a *TCP/IP* port.

C. IC Peripheral Circuit Design



Power line interface circuit

The power line interface circuit ofST7538 composed of an isolation transformer and two band-pass filters for passing the carrier frequency signal. the left Tx band-pass filter is in charge of high-side cut-off frequency, and the right Tx band-pass filter is in charge of low-side cut-off frequency.

The power line impedance should be known to design the isolation transformer. the impedance range for the carrier frequency is roughly 1'"100[ohm].

The bandwidth of the band-pass filter is 60[kHz] centring the carrier frequency,132.5[kHz]. In practice, the two cut-off frequencies are101.9[kHz] and 156.7[kHz], respectively

5.2 EXPERIMENTAL RESULTS

Several PLC modules are manufactured and then applied to the rainwater monitoring system.

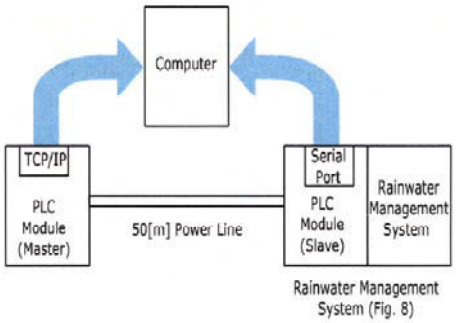


Fig. 5: Experimental configuration

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Fig 5.demonstrate the operation of the PLC modules. The connecting line between two modules is the electric power line utilized the communication wire in PLC. The distance from the master module to the slave one is50[m]. At first, a data is transferred to the main PLC module from computer. Then, the main PLC module conveys the data to the slave PLC module through the long power line. The slave
PLC module transmits the receiving data to the computer immediately.

VI. PERFORMANCE OF POWER LINE COMMUNICATION SYSTEMS WITH NOISE REDUCTION SCHEME FOR SMART GRID APPLICATIONS

Power line communication is a leading techniques over a smart grid because of several features like a less installation cost since power line is available everywhere. In smart grid lots of devices are actives at a time which causes multipath environment. Also some noise are generated which has to reduce. The techniques we are using to reduce the noise are clipping scheme and equalizer**.** Clipping is cutting off amplitude of the received signal over threshold level and the equalizer compensates effects of PLC channel.

6.1 NOISE MODEL:

The fig. illustrates a noise block diagram in PLC channel. The signal $s(t)$ is transmitted over PLC channel with the
impulse response $h(t)$ and the various noises added to the signal passed the channel. Then, the received signal $r(t)$ is
arrived at the receiver. The noises can be typified into five categories: coloured background noise, narrow-band noise ,periodic impulsive noise synchronous or asynchronous to the main frequency (50~60Hz), and asynchronous a periodic impulsive noise.

Some noise among them rarely has properties similar to the easily analyzed white Gaussian noise of the receiver. The background, narrow-band, and periodic asynchronous noise may be summarized as background noise since their properties are typically stationary over periods of seconds and minutes or sometimes even for hours. However, asynchronous impulsive noise and periodic synchronous impulsive noise are varying rapidly for microseconds to

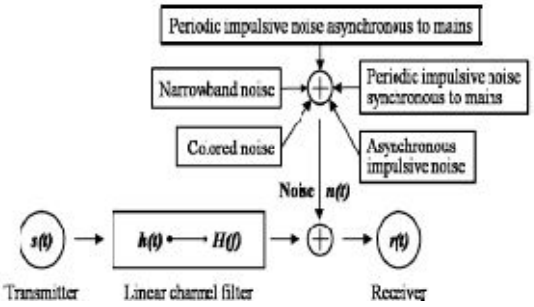
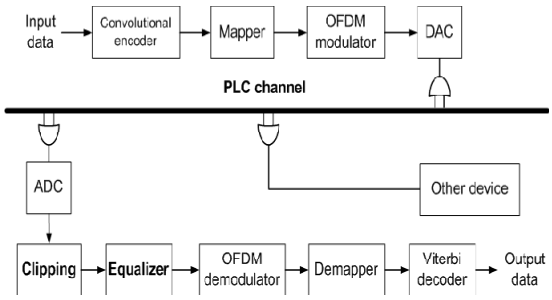


Fig.6: noise model

milliseconds. Therefore, it is necessary to set up impulsive noise model. To establish impulsive noise model, we consider Middleton's Class *A* noise mode. For the Class *A* noise model the observed process is assumed to have two independent components:

$$z(t) = z_G(t) + z_P(t).$$

The first term, $zG(t)$, is a stationary background Gaussian noise component.



Block diagram of proposed PLC system model.

6.2 SYSTEM MODEL

PLC system model considered in this paper is illustrated in fig. Binary data stream is modulated by channel coding at the convolution encoder. The channel coding compensates for the effect of channel fading. Then, the phase shift keying (PSK) modulated signal is changed serial signal to a number of parallel frames. Each frame is loaded subcarriers and summed up through inverse fast Fourier transform (IFFT). This signal is converted to analog at the digital-to-analog one of the promising candidates for smart grid, power line communication (PLC) is a leading technique because of its advantages.converter (DAC) and then transmitted via power lines. The received signal experienced a variety of noises changed to digital signal again at the analog-to-digital converter (ADC).

Next, channel and impulsive noise are mitigated through the clipping and equalizer block. Finally, the received signal is recovered as the original data stream via FFT and demodulator.In this paper, we employed the
multipath channel model proposed in, and its impulse response is given as

$$H(f) = \sum_{i=1}^{N} g_i \cdot e^{-(a_o + a_1 f^k)d_i} \cdot e^{-j2\pi f(d_i / v_p)}$$

where, g_i is weighting term, $e^{-(a_0+a_1 f^k)d_i}$ is attenuation and $e^{-j2\pi f(d_i/v_p)}$ is delay term.

NOISE REDUCTION SCHEME

A. ZF Receiver

In order to reject the interference, we consider the zero forcing (ZF) linear detectors which satisfy the condition
shown below.

$$W_{ZF} H = I,$$

where $W_{ZF} = \left(H^H H\right)^{-1} H^H$ is the ZF decoding matrix, Denotes Hermitian transpose, H is channel matrix and I is identity matrix. The receiver can obtain the estimated signal by using ZF equalization, which is given by

$$\hat{X} = W_{ZF} Y,$$

Where $\hat{X}$ is an estimate matrix of the transmitted signal.
The ZF algorithm is ideal when the channel is noiseless. However, when the channel is noisy, the ZF algorithm will amplify the noise greatly where the channel has small magnitude in the attempt to invert the channel completely.

B. Clipping Technique

The orthogonal frequency division multiplexing (OFDM) signal with long symbol period is more robust to impulsive noise because the impulse noise energy is spread over N subcarriers. If techniques mitigating impulsive noise, however, are not considered, it can still significantly affect the performance of OFDM systems, especially in a hostile medium such as power lines. In order to overcome the effect of impulsive noise, clipping technique is often employed in practical applications owing to its simplicity [17]. A clipping block is used at the front-end of OFDM receiver before demodulating. The most attractive point is that clipping changes only the amplitude of the signal over specific threshold level without changing its phase. Therefore, the received signal with clipping can be expressed as below.

$$y_n = \begin{cases} r_n & |r_n| \le T_c \\ T_c e^{j\arg(r_n)} & |r_n| > T_c \end{cases}, \quad n = 0,1,\cdots,N-1,$$

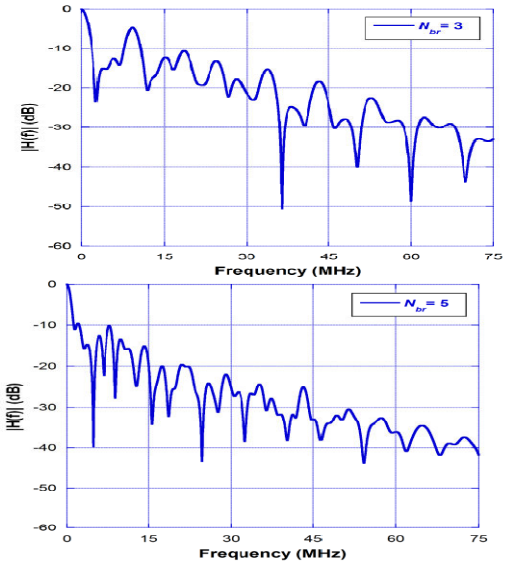
Where *Tc* denote the clipping threshold.

SIMULATION RESULTS

In the paper, the size of data frame and CP length is 3072 and 336 samples each, and 30 packets are transmitted. Simulation is conducted at the case that the number of power line branches *Nbr*is 3 and 5. The clipping scheme and equalizer are applied to all of the case. As an equalizer, ZF scheme is used.

Channel Response:

Fig. illustrate channel responses. As we mentioned above, PLC channels suffers from frequency selective fading. It can be also confirmed the magnitude of the channel is attenuated as the frequency increases. Also, as the number of branches increase, the channel state is getting poor because the reflection between devices and lines or branch lines and main lines often occurs.



VII. CONCLUSION

As more and more industries become computerized, industrial automation is a major topic of research in the country now. It is mainly focused on the interconnection of the all the devices and bidirectional flow of data occurring between all. The usage of power line carrier communication has major advantages like most important criteria of money saving. . In large industries wiring for controlling of any device will consume time, space, energy and money. So the using of the existing resource "the existing power line" is the ideal way. Existing protocols have been used for data transfer. The future of PLC is bright. It can be extensively used in industrial security and automation. Adittionally, Plcc can be used in "Railway bogie appliances" .

Also it proves to be a better alternative to home networking and in near future it will be commercially available due to its low cost and high speed with less power loss.

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MODELING & SIMULATION OF MITIGATION OF VOLTAGE FLICKER IN DISTRIBUTION SYSTEM USING DSTATCOM BY VARYING LOADS

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Lords Institute of Engineering and Technology

Abstract:-This paper demonstrates an effective control technique for a Distribution Static Compensator. A Distribution Static Synchronous Compensator (D-STATCOM) is used to regulate voltage on a 25-kV distribution network. Two feeders (21 km and 2 km) transmit power to loads connected at buses B2 and B3. A shunt capacitor is used for power factor correction at bus B2. The 600-V load connected to bus B3 through a 25kV/600V transformer represents a plant absorbing continuously changing currents, similar to an arc furnace, thus producing voltage flicker. The variable load current magnitude is modulated at a frequency of 5 Hz so that its apparent power varies approximately between 1 MVA and 5.2 MVA, while keeping a 0.9 lagging power factor. This load variation will allow you to observe the ability of the D-STATCOM to mitigate voltage flicker.

Index Terms – *Voltage Fluctuation, DSTATCOM, Custom Power Devices, Power Quality, MATLAB.*

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INTRODUCTION

In the early days of power transmission in the late 19th century problems like voltage deviation during load changes and power transfer limitation were observed due to reactive power unbalances. Today these Problems have even higher impact on reliable and secure power supply in the world of Globalization and Privatization of electrical systems and energy transfer. The development in fast and reliable semiconductors devices (GTO and IGBT) allowed new power electronic Configurations to be introduced to the tasks of power Transmission and load flow control. The FACTS devices offer a fast and reliable control over the transmission parameters, i.e. Voltage, line impedance, and phase angle between the sending end voltage and receiving end voltage[1].

Most widely known custom power devices are DSTATCOM, UPQC, DVR among them DSTATCOM is very well known and can provide cost effective solution for the compensation of reactive power and unbalance loading in distribution system. Among these control schemes instantaneous reactive power theory and synchronous rotating reference frame are most widely used[2]. This paper focuses on the compensating the voltage sag, swells and momentary interruptions. The dynamic performance is analyzed and verified through simulation.

Mitigation of the arc furnace flicker using the voltage source converter based shunt mitigation devices, (such as DSTATCOMs and STATCOMs), depends mainly on the vector control scheme[3]. In this control scheme, the voltage profile is stabilized by injecting adequate reactive and/or real power using DSTATCOM and STATCOM . This control scheme that dominates the custom power conditioner utilizes the decoupled d-q vector control, in which the direct and quadrature currents of the DSTATCOM are compared with particular set-values and the difference is controlled by a PI controller to stabilize the voltage at the point of installation .

The main objective of the paper is that causes of power quality problems are generally complex and difficult to detect[4]. Technically speaking, the ideal AC line supply by the utility system should be a pure sine wave of fundamental frequency (50/60Hz).Different power quality problems, their characterization methods and possible causes are discussed above and which are responsible for the lack of quality power which affects the customer in many ways. We can therefore conclude that the lack of quality power can cause loss of production, damage of equipment or appliances or can even be detrimental to human health. It is therefore imperative that a high standard of power quality is maintained[5].

The DSTATCOM is controlled using different control theories like the phase shift theory and the decoupled theory using the PI controller.

SYSTEM CONFIGURATION

The system under study is illustrated in Fig. 1. This system is part of a real distribution system. The developed control is employed to operate the DSTATCOM in order to inject a certain reactive power that is equivalent to the reactive power consumed by the arc furnace[6].

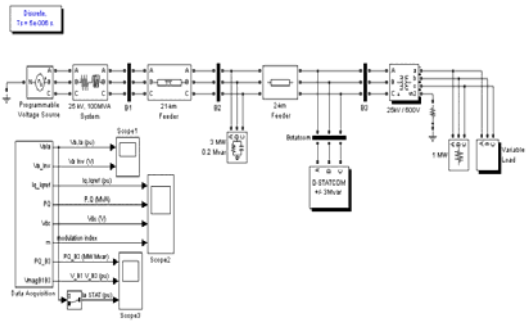


Fig 1: Main Circuit for the DSTATCOM connected to 25kv

Distribution system

DSTATCOM is most effective devices to solve many power quality problems. The device have voltage source converter in it, and the operation of this voltage source converter is depends on the switching pulses of IGBT gates. Till today there are so many control schemes are proposed for the control of voltage source converter. In this work a direct voltage controller is simulated for control of switching pulses for DSTATCOM[7].

A. Simulation of DSTATCOM:

In this paper, the performance of VSC based power devices acting as a voltage controller is investigated. Moreover, it is assumed that the converter is directly controlled (i.e., both the angular position and the magnitude of the output voltage are controllable by appropriate on/off signals) for this it requires measurement of the rms voltage and current at the load point[8].

B. Distribution Static Compensator (D-STATCOM):

The DSTATCOM is commonly used for voltage sags mitigation and harmonic elimination at the point of connection. The DSTATCOM employs the same blocks as the DVR, but in this application the coupling transformer is connected in shunt with the ac system. The VSC generates a three-phase ac output current which is controllable in phase and magnitude. These currents are injected into the ac distribution system in order to maintain the load voltage at the desired voltage reference. Active and reactive power exchanges between the VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1) Voltage regulation and compensation of reactive power;
2) Correction of power factor
3) Elimination of current harmonics.

In this DSTATCOM implementation, a voltage-source inverter converts a dc voltage into a three-phase ac voltage that is synchronized with, and connected to, the ac line through a small tie reactor and capacitor (ac filter).The block diagram of the Distribution Static Compensator is shown in figure below.

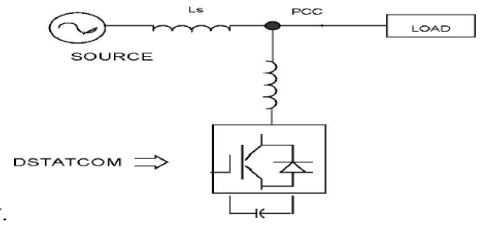


Fig.1.2.block diagram of DSTATCOM circuit

C. DSTATCOM components:

DSTATCOM involves mainly three parts

IGBT or GTO based dc-to-ac inverters:

These inverters are used which create an output voltage wave that's controlled in magnitude and phase angle to produce either leading or lagging reactive current, depending on the compensation required[9].

L-C filter:

The LC filter is used which reduces harmonics and matches inverter output impedance to enable multiple parallel inverters to share current. The LC filter is chosen in accordance with the type of the system and the harmonics present at the output of the inverter.

Control block:

Control block is used which switch Pure Wave DSTATCOM modules as required. They can control external devices such as mechanically switched capacitor banks too. These control blocks are designed based on the various control theories and algorithms like instantaneous PQ theory, synchronous frame theory etc.

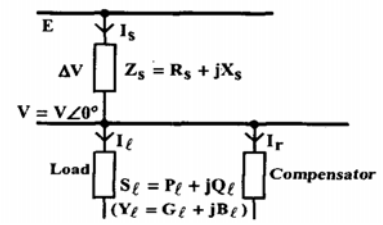
D. Principle of DSTATCOM of Voltage Regulation:

a: voltage regulation without compensator:-

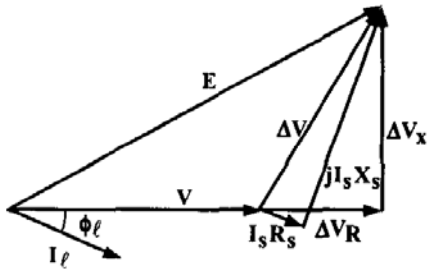
Voltage E and V mean source voltage and PCC voltage respectively. Without a voltage compensator, the PCC voltage drop caused by the load current, I_l is as shown in fig.3.3.3 (b) as ΔV

$$I_S = I_L + I_R$$

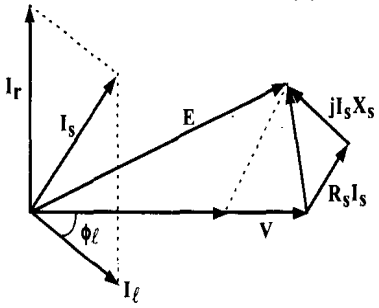
Where I_R is the compensating current



(a)



(b)



(c)

Fig.1.3 (a) the equivalent circuit of load and supply system
(b) Phasor of uncompensated line
(c) Phasor of the compensated line

$$\Delta V = E - V = Z_S I_L$$

$$S = VI^*,\ S\_ = V^*I$$

From above equation

$$I_L = \left(\frac{P_L - jQ_L}{V} \right)$$

So that

$$\Delta V = (R_S + j X_S)\left(\frac{P_L - jQ_L}{V} \right)$$

$$= \left(\frac{R_S P_L - X_S Q_L}{V} \right) + J\left(\frac{X_S P_L + R_S Q_L}{V} \right)$$

$$= \Delta V_R + \Delta V_X$$

The voltage change has a component ΔV_R in phase with V and a component ΔV_x , in quadrature with V, which are illustrated in fig1.3(b). it is clear that both magnitude and phase of V , relative to the supply voltage E, are the functions magnitude and phase of load current, namely voltage drop depends on the both the real and reactive power of the load[10]. The component ΔV can be written as

$$\Delta V = I_S R_S - jI_S X_S$$

b: voltage regulation using the DSTATCOM:-

Fig.1.3. (c) shows the vector diagram with voltage compensation. By adding a compensator in parallel with the load, it is possible to make $|E| = |V|$ by controlling the current of the compensator.

$$I_S = I_L + I_R$$

Where I_R is compensator current

CONTROL ALGORITHM

For reactive power compensation, DSTATCOM provides reactive power as needed by the load and therefore the source current remains at unity power factor (UPF). Since only real power is being supplied by the source, load balancing is achieved by making the source reference current balanced[11]. The reference source current used to decide the switching of the DSTATCOM has real fundamental frequency component of the load current which is being extracted by these techniques.

1. Phase Shift Control
2. Decoupled Current Control (p-q theory)

A. Phase Shift Control

In this control algorithm the voltage regulation is achieved in a DSTATCOM by the measurement of the rms voltage at the load point and no reactive power measurements are required. Fig.2 shows the block diagram of the implemented scheme.

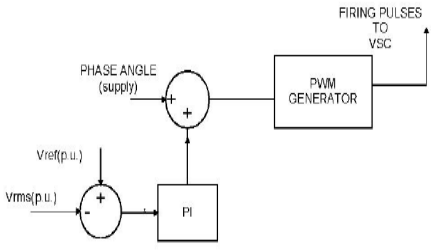


Fig 2. block diagram of phase shift control

B. Decoupled Current Control or instantaneous p-q theory

This algorithm requires the measurement of instantaneous values of three phase voltage and current. Fig.4.2.1. shows the block diagram representation of the control scheme[12]. The

compensation is achieved by the control of id and iq. Using the definition of the instantaneous reactive power theory for a balanced three phase three wire system, the quadrature component of the voltage is always zero, the real (p) and the reactive power (q) injected into the system by the DSTATCOM can be expressed under the dq reference frame as:

$$\mathbf{p = v_d i_d + v_q i_q}$$
$$\mathbf{q = v_q i_d - v_d i_q}$$

Since vq=0, id and iq completely describe the instantaneous value of real and reactive powers produced by the DSTATCOM when the system voltage remains constant. Therefore the instantaneous three phase current measured is transformed by abc_ to_dqo transformation. The decoupled d-axis component id and q axis component iq are regulated by two separate PI regulators. The instantaneous id reference and the instantaneous iq reference are obtained by the control of the dc voltage and the ac terminal voltage measured. Thus, instantaneous current tracking control is achieved using four PI regulators[13]. A Phase Locked Loop (PLL) is used to synchronize the control loop to the ac supply so as to operate in the abc_to_dqo reference frame.

The instantaneous active and reactive powers p and q can be decomposed into an average and an oscillatory component

$$p = \bar{p} + \tilde{p}$$
$$q = \bar{q} + \tilde{q}$$

Where $\bar{p}$ and q are the average part and $\tilde{p}$ and $\tilde{q}$ are oscillatory part of real and reactive instantaneous powers. The compensating currents are calculated to compensate the instantaneous reactive power and the oscillatory component of the instantaneous active power[14]. In this case the source transmits only the non-oscillating component of active power.

Therefore the reference source currents $i^*_{s\alpha}$ and $i^*_{s\beta}$ in α-β coordinate are expressed as:

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \frac{1}{\Delta}\begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix}\begin{bmatrix} \bar{p} \\ 0 \end{bmatrix}$$

These currents can be transformed in a-b-c quantities to find the reference currents in a-b-c coordinate[15]

.

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i_o \\ i_\alpha \\ i_\beta \end{bmatrix}$$

Where i_o is the zero sequence components which is zero in 3-phase 3-wire system

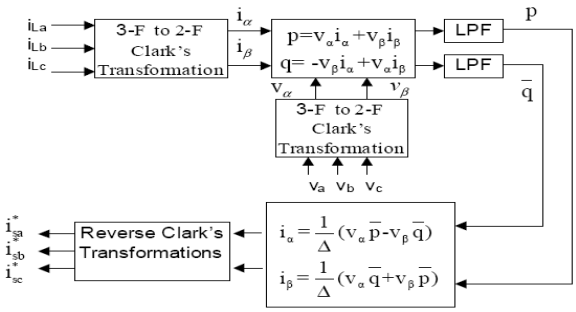


Fig.3. block diagram of decoupled theory based control of DSTATCOM

SIMULATION RESULTS

The simulation results are shown below for the fig 1 (i.e The main circuit for the DSTSTCOM connected to 25 KV distribution network)

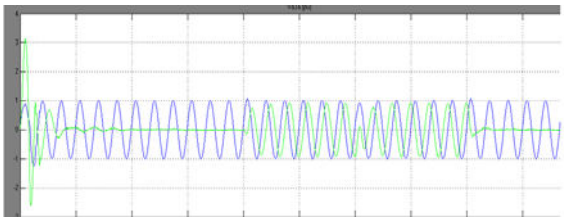


Fig.6. Load Side Phase Voltage and Phase Current VaI,a(Pu)

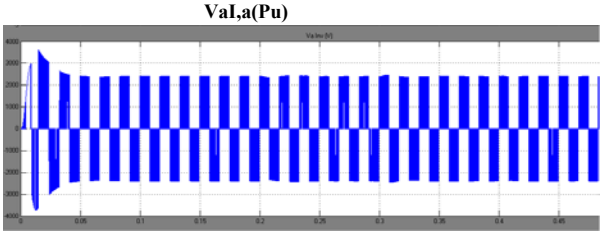


Fig 7: Load side phase Voltage and Inverse VoltageVa Inv (V)

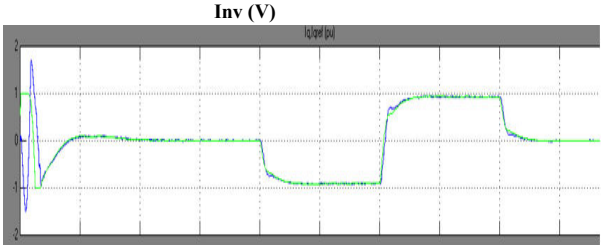


Fig 8: Quadrature Axis Current Iq And Reference current,Iref (pu) at Load Side

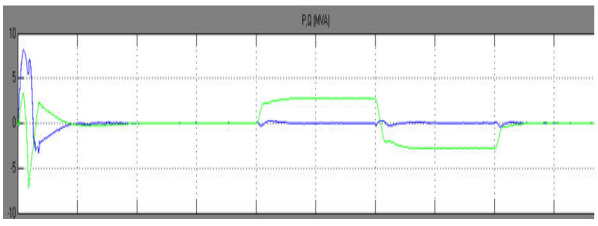


Fig 9:Load side Active Power & Reactive Power P,Q (MVA)

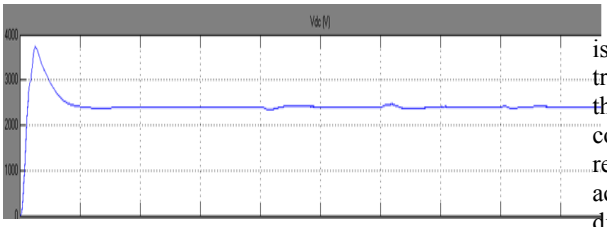


Fig 10: DC Voltage Vdc (V) at Load side

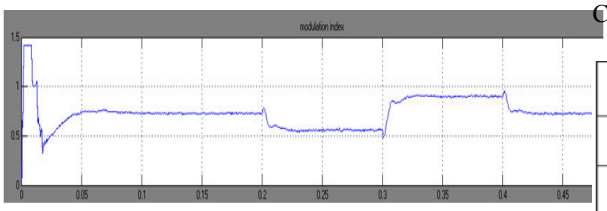


Fig 11: Load Side Modulation Index

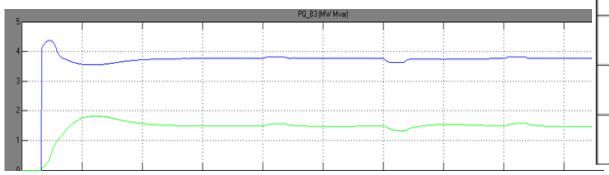


Fig 12: Reactive Power & Active Power PQ (MW Mvar) at bus 3

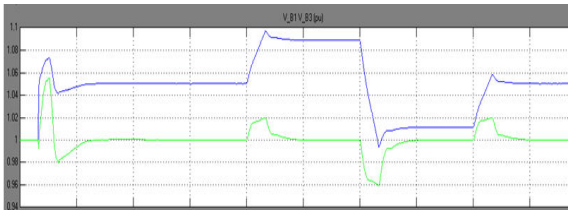


Fig 13: Voltage Wave form at Bus 1 & Bus 3 (pu)

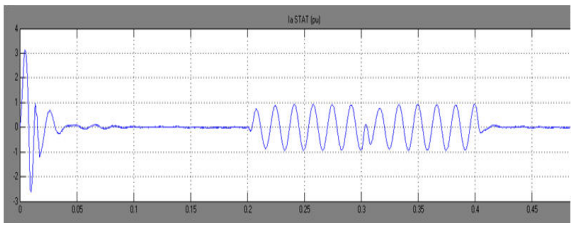


Fig 14: STATCOM Phase Current Ia (Pu)

CONCLUSION

CUSTOM POWER (CP) devices can be used, at reasonable cost, to provide high power quality and improved power service. These Custom Power devices provide solutions to power quality at the medium voltage distribution network level. This paper presents the detailed modeling of one of the custom power products, DSTATCOM is presented and also a comparative study of two control algorithms, phase shift control and instantaneous P-Q theory, used for the control of DSTATCOM are discussed with their relative merits and demerits.

It is concluded that a DSTATCOM though is conceptually similar to a STATCOM at the transmission level; its control scheme should be such that in addition to complete reactive power compensation, power factor correction and voltage regulation the harmonics are also checked, and for achieving improved power quality levels at the distribution end.

COMPARISION OF CONTROL ALGORITHMS:

Algorithms Parameters	Phase Shift Control	Decoupled Current Control
Reactive Power Compensation	Partial	Complete
Performance under balanced and nonlinear loads	Contains undesired harmonics in case of nonlinear load	Satisfactiory in case of linear loads
Applicable for Single Phase Systems	Yes	No
Total Harmonic Distortion (THD)	-	Much higher than 5%
PWM Switching Frequency	Fixed	Fixed

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MODELING & SIMULATION OF FAULT DETECTION AND TIGATION IN MULTILEVEL CONVERTER STATCOM

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Abstract:- Many static synchronous compensators (STATCOMs) utilize multilevel converters due to the following: 1) Lower harmonic injection into the power system; 2) Decreased stress on the electronic components due to decreased voltages; and 3) Lower switching losses. One disadvantage, however, is the increased likelihood of a switch failure due to the increased number of switches in a multilevel converter. A single switch failure, however, does not necessarily force an (2n + 1)-level STATCOM
offline. Even with a reduced number of switches, a STATCOM can still provide a significant range of control by removing the module of the faulted switch and continuing with (2n − 1) levels. This approach introduces an approach to detect the existence of the faulted switch, identify which switch is faulty, and reconfigure the STATCOM. This approach is illustrated on an eleven-
level STATCOM and the effect on the dynamic performance and the total harmonic distortion (THD) is analyzed

Index Terms *– Fault detection, multilevel converter, static synchronous compensator (STATCOM).*

I. INTRODUCTION

The static synchronous compensator (STATCOM) has been well accepted as a power system controller for improving voltage regulation and reactive compensation. There are several compelling reasons to consider a multilevel converter topology for the STATCOM. These well known reasons include the following: 1) lower harmonic injection into the power system; 2) decreased stress on the electronic components due to decreased voltages; and 3) lower switching losses. Various multilevel converters also readily lend themselves to a variety of PWM strategies to improve efficiency and control. An eleven-level cascaded multilevel STATCOM is shown in Fig. 1. This converter uses several full bridges in series to synthesize staircase waveforms. Because every full bridge can have three output voltages with different switching combinations, the number of output voltage levels is 2n + 1 where n is the number of full bridges in every phase. The converter cells are identical and therefore modular.

As higher level converters are used for high output rating power applications, a large number of power switching devices will be used. Each of these devices is a potential failure point. Therefore, it is important to design a sophisticated control to produce a fault-tolerant STATCOM. A faulty power cell in a cascaded H-Bridge STATCOM can potentially cause switch modules to explode leading to the fault conditions such as a short circuit or an overvoltage on the power system resulting in an expensive down time. Subsequently, it is crucial to identify the existence and location of the fault for it to be removed

Fig. 1. Eleven-level cascaded multilevel STATCOM.

Several fault detection methods have been proposed over the last few years. Resistor sensing, current transformation and VCE sensing are some of the more common approaches. For example, a method based on the output current behavior is used to identify IGBT short circuits. The primary drawback with the proposed approach is that the fault detection time depends on the time constant of the load. Therefore, for loads with a large RL time constant, the faulty power cell can go undetected for numerous cycles, potentially leading to circuit damage. another fault detection approach proposed is based on a switching frequency analysis of the output phase voltage. his method was applied to flying capacitor converters and has not been extended to cascaded converters. AI-based methods were proposed to extract pertinant signal features to detect faults in sensors are used to measure each IGBT current and to initiate switching if a fault is detected. A fault-tolerant neutral point- clamped converter was proposed. In a reconfiguration system based on bidirectional switches has been designed for three- phase asymmetric cascaded H-bridge inverters. The fundamental output voltage phase shifts are used to rebalance a faulted multilevel cascaded converter. In this method requires only that the output dc link voltage of each phase be measured. This measurement is typically accomplished anyway for control purposes. If a fault is detected, the module in which the fault occurred is then isolated and removed from service. This approach is consistent with the modular design of cascaded converters in which the cells are designed to be interchangeable and rapidly removed and replaced. Until the module is replaced, the multilevel STATCOM continues to operate with slightly decreased, but still acceptable, performance.

In summary, this approach offers the following advantages:
- No additional sensing requirements;
- Additional hardware is limited to two by-pass switches per
module;
- is consistent with the modular approach of cascaded multilevel converters; and
- The dynamic performance and THD of the STATCOM is not significantly impacted.

II. FACTS

Flexible ac transmission systems, called facts, got in the recent years a well known term for higher controllability in power systems by means of power electronic devices. Several facts-devices have been introduced for various applications worldwide. A number of new types of devices are in the stage of being introduced in practice. In most of the applications the controllability is used to avoid cost intensive or landscape requiring extensions of power systems, for instance like upgrades or additions of substations and power lines. Facts-devices provide a better adaptation to varying operational conditions and improve the usage of existing installations. The basic applications of facts-devices are: Power flow control, Increase of transmission capability, Voltage control, Reactive power compensation, Stability improvement, Power quality improvement, Power conditioning, Flicker mitigation, Interconnection of renewable and distributed generation and storages. Figure 3 shows the basic idea of facts for transmission systems. The usage of lines for active power transmission should be ideally up to the thermal limits. Voltage and stability limits shall be shifted with the means of the several differentfacts devices. It can be seen that with growing line length, the opportunity for facts devices gets more and more important. The influence of facts-devices is achieved through switched or controlled shunt compensation, series compensation or phase shift control. The devices work electrically as fast current, voltage or impedance controllers. The power electronic allows very short reaction times down to far below one second.

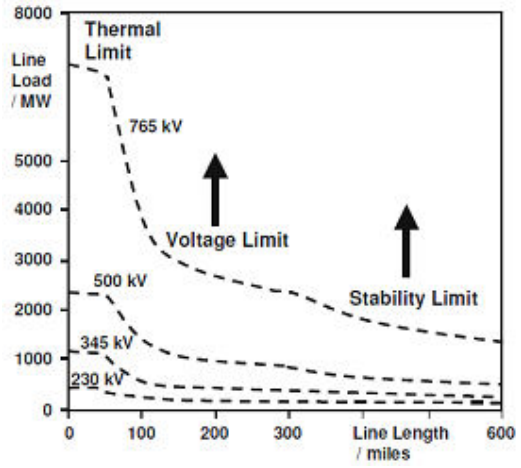

Fig 2 a number of basic devices separated into the conventional ones

The development of facts-devices has started with the growing capabilities of power electronic components. Devices for high power levels have been made available in converters for high and even highest voltage levels. The overall starting points are network elements influencing the reactive power or the impedance of a part of the power system. Figure 2 shows a number of basic devices separated into the conventional ones and the facts-devices. For the facts side the taxonomy in terms of 'dynamic' and 'static' needs some explanation. The term 'dynamic' is used to express the fast controllability of facts-devices provided by the power electronics. This is one of the main differentiation factors from the conventional devices. The term 'static' means that the devices have no moving parts like mechanical switches to perform the dynamic controllability. Therefore most of the facts-devices can equally be static and dynamic.

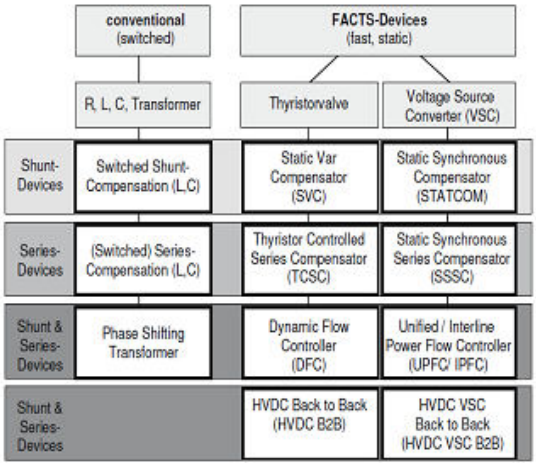

Fig3. Overview of major FACTS-Devices

The left column in figure 2 contains the conventional devices build out of fixed or mechanically switch able components like resistance, inductance or capacitance together with transformers. The facts-devices contain these elements as well but use additional power electronic valves or converters to switch the elements in smaller steps or with switching patterns within a cycle of the alternating current. The left column of facts-devices uses thyristor valves or converters. These valves or converters are well known since several years. They have low losses because of their low switching frequency of once a cycle in the converters or the usage of the thyristors to simply bridge impedances in the valves. The right column of facts-devices contains more advanced technology of voltage source converters based today mainly on insulated gate bipolar transistors (IGBT) or insulated gate commutated thyristors (IGCT). Voltage source converters provide a free controllable voltage in magnitude and phase due to a pulse width modulation of the IGBTS or IGCTS. High modulation frequencies allow to get low harmonics in the output signal and even to compensate disturbances coming from the network. The disadvantage is that with an increasing switching frequency, the losses are increasing as well. Therefore special designs of the converters are required to compensate this.

III.MODELING OF CASE STUDY

A. Multilevel STATCOM:

A cascaded multilevel STATCOM contains several H-bridges in series to synthesize a staircase waveform. The inverter legs are identical and are therefore modular. In the eleven-level STATCOM, each leg has five H-bridges. Since each full bridge generates three different level voltages (V, 0,−V) under different switching states, the number of output voltage levels will be eleven. A multilevel configuration offers several advantages over other converter types.

1) It is better suited for high-voltage, high-power applications than the conventional converters since the currents and voltages across the individual switching devices are smaller.

2) It generates a multistep staircase voltage waveform approaching a more sinusoidal output voltage by increasing the number of levels.
3) It has better dc voltage balancing, since each bridge has its own dc source.

To achieve a high-quality output voltage waveform, the voltages across all of the dc capacitors should maintain a constant value. Variations in load cause the dc capacitors to charge and discharge unevenly leading to different voltages in each leg of each phase. However, because of the redundancy in switching states, there is frequently more than one state that can synthesize any given voltage level. Therefore, there exists a "best" state among all the possible states that produces the most balanced voltages. Since there are multiple possible switching states that can be used to synthesize a given voltage level, the particular switching topology is chosen such that the capacitors with the lowest voltages are charged or conversely, the capacitors with the highest voltages are discharged. This redundant state selection approach is used to maintain the total dc link voltage to a near constant value and each individual cell capacitor within a tight bound. Different pulse width modulation (PWM) techniques have been used to obtain the multilevel converter output voltage. One common PWM approach is the phase shift PWM (PSPWM) switching concept. The PSPWM strategy causes cancellation of all carrier and associated sideband harmonics up to the (N − 1) th carrier group for an N-level converter. Each carrier signal is phase shifted by

$$\Delta\phi = \frac{2\pi}{n} \qquad (1)$$

Where n is the number of cells in each phase. Fig. 4 illustrates the carrier and reference waveforms for a phase leg of the eleven-level STATCOM. In this figure, the carrier frequency has been decreased for better clarity. Normally, the carrier frequency for PWM is in the range of 1–10 kHz.

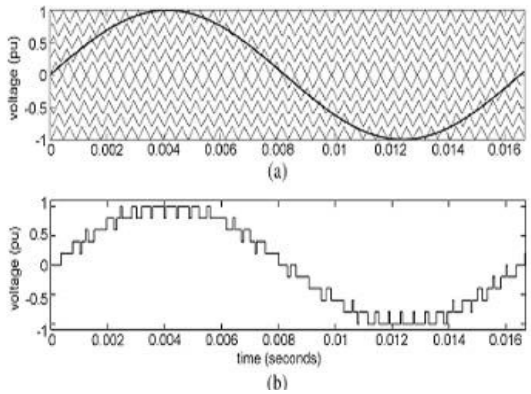

Fig 4. (a) Carrier and reference waveform for PSPWM. (b) Output waveform.

B. fault analysis for the multilevel STATCOM:
A converter cell block, as shown in Fig. 5, can experience several types of faults. Each switch in the cell can fail in an open or closed state. The closed state is the most severe failure since it may lead to shoot through and short circuit the entire cell. An open circuit can be avoided by using a proper gate circuit to control the gate current of the switch during the failure.

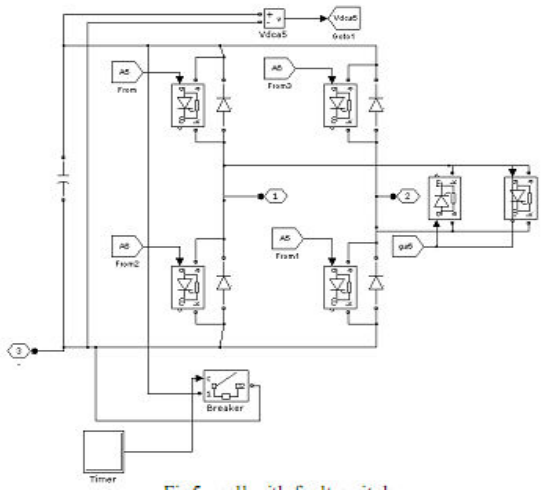

Fig5. cell with fault switch

If a short circuit failure occurs, the capacitors will rapidly discharge through the conducting switch pair if no protective action is taken. Hence, the counterpart switch to the failed switch must be quickly turned off to avoid system collapse due to a sharp current surge. Nomenclature for the proposed method is given in Table I.

TABLE I NOMENCLATURE

E_{out}	STATCOM output voltage (V)
$\hat{E}_{out}$	Filtered STATCOM output voltage (RMS) (V)
E'	STATCOM threshold voltage (constant) (V)
S_{j1}, S_{j2}	Switching signal of the j-th cell (0, 1)
f_i	possible STATCOM output voltage (V)
x_i	difference between possible and actual STATCOM output (V)
g_j	bypass signal for j-th cell (0, 1)

The staircase voltage waveform shown in Fig. 4 is synthesized by combining the voltages of the various cells into the desired level of output voltage. At the middle levels of the voltage waveform, due to the switching state redundancy, there are more than one set of switching combinations that may be used to construct the desired voltage level. Therefore, by varying the switching patterns, the loss of any individual cell will not significantly impact the middle voltages of the output voltage. However, the peak voltages require that all cells contribute to the voltage; therefore, the short circuit failure of any one cell will lead to the loss of the first and (2n+ 1) output levels and cause degradation in theability of the STATCOM to produce the full output voltage level.

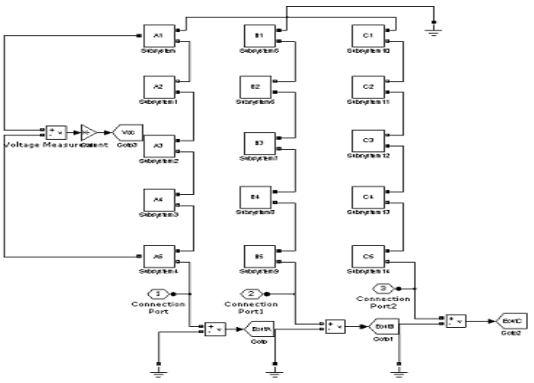

Fig6. Multilevel converter STATCOM

Consider the simplified eleven-level converter shown in Fig. 6. The process for identifying and removing the faulty cell block is summarized in Fig. 8. The input to the detection algorithm is Êout for each phase, where Êout is the STATCOM filtered RMS output voltage. If the STATCOM RMS output voltage drops below a preset threshold value (E'), then, a fault is known to have occurred.

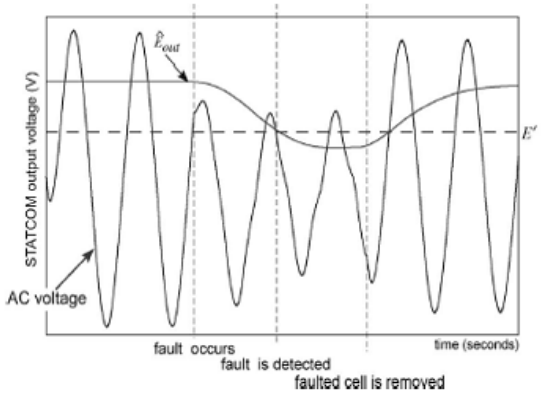

Fig.7 STATCOM-filtered output voltage and threshold value

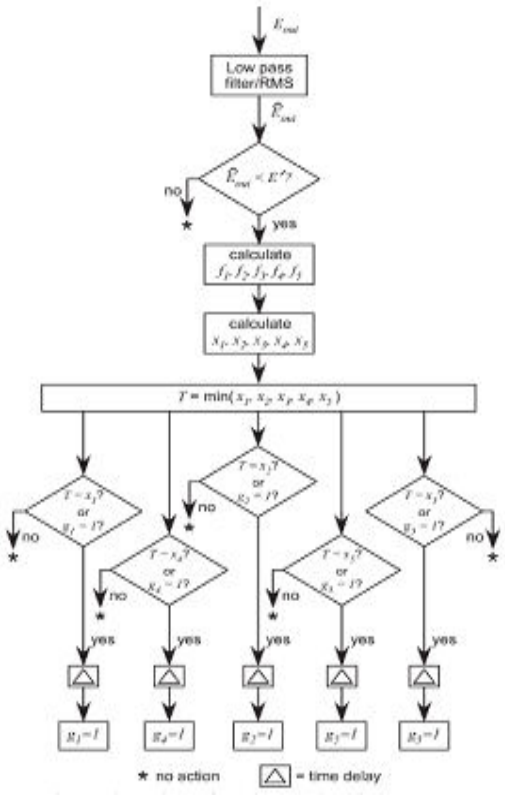

Fig8. Flowchart for eleven-level converter.

Once a fault has been detected to have occurred, then, the next step is to identify the faulty cell. By utilizing the switching signals in each converter cell, (i.e., S1 and S2), it is possible to calculate all of the possible voltages that can be produced at any given instant as illustrated in Table II (terminology adopted)

SWITCHING STATE AND OUTPUT VOLTAGE OF AN H-BRIDGE

S_1	S_2	v_{ax}^{+}	v_{ax}^{-}	v_{ax}
0	0	0	0	0
0	1	0	v_{dc}	$-v_{dc}$
1	0	v_{dc}	0	v_{dc}
1	1	v_{dc}	v_{dc}	0

(Cell 1 faulted)

$$f_2 = V_{dc0}(S_{11} - S_{12} + S_{31} - S_{32} + S_{41} - S_{42} + S_{51} - S_{52})$$

(Cell 2 faulted)

$$f_5 = V_{dc0}(S_{11} - S_{12} + S_{21} - S_{22} + S_{31} - S_{32} + S_{41} - S_{42})$$

(Cell 5 faulted) (2)

Or more succinctly as

$$f_i = V_{dc0} \sum_{\substack{j=1 \\ j \neq i}}^{n} (S_{j1} - S_{j2}), \qquad i = 1, \ldots, n \tag{3}$$

Where V_{dc0} is the ideal voltage across a single cell block. If there is a faulted cell, only one f_i will be near the actual STATCOM output phase voltage E_{out}; all of the others will be too high. Therefore, to determine the location of the fault cell, each f_i is compared against E_{out} to yield

$$x_i = |E_{out} - f_i|, \qquad i = 1, \ldots, n. \tag{4}$$

The smallest xi indicates the location of the faulted block because this indicates the f_i which most closely predicts the actual E_{out}. The choice of threshold voltage E' depends on the number of cells in the converter. The ideal output voltage is

$$\hat{E}_{out,0} = \frac{nV_{dc0}}{\sqrt{2}}. \tag{5}$$

During a fault, E_{out} will decrease by V_{dc0} yielding

$$\hat{E}_{out,fault} = \frac{(n-1)V_{dc0}}{\sqrt{2}} = \frac{n-1}{n}\hat{E}_{out,0}. \tag{6}$$

Therefore, the threshold voltage E' should be chosen such that $(n - 1/n)\ E_{out,0} \leq E' \leq E_{out,0}$. In an eleven-level converter, $n = 5$ and the faulted RMS voltage will decrease by roughly 20%. Therefore, a good choice for E' is 85% of the rated output STATCOM voltage. The last step is to actuate the module bypass switch g_i shown in Fig. 5. A slight time delay is added to the logic to neglect for momentary spikes that may occur. It is desirable to neglect momentary sags in the dc link voltage, but respond to sags of increased duration that indicate a faulted module. Fig. 711shows the realization logic for the proposed fault detection and module removal method. The use of a fault handling switch in multilevel converters is not uncommon. In, a fault handling switch is used in a flying capacitor multilevel inverter. While the additional circuitry does increase the cost of the circuit, it also increases the reliability be enabling the circuit to keep working (albeit at a slightly reduced operating range) until the module can be replaced.

IV. MATLAB DESIGN OF CASE STUDY AND RESULTS

The single line diagram of the electrical distribution system feeding an arc furnace is shown in Fig. 9. The STATCOM has been shown to be an efficient controller to mitigate arc furnace flicker [27]. The electrical network consists of a 115-kVgenerator and an impedance that is equivalent to that of a large network at the point of common coupling (PCC). The STATCOM is connected to the system through a Y-Delta transformer. The system was simulated using

PSCAD/ EMDTC.The electrical arc furnace load is nonsinusoidal, unbalanced,and randomly fluctuating. Electric arc furnaces are typicallyused to melt steel and will produce current harmonics thatare random. In addition to the integer harmonics, arc furnacecurrents are rich in interharmonics [24]. The flicker waveform has subsynchronous variations in the 5–35-Hz range [25]. Fig.12 shows the active power drawn by the arc furnace. Note that the STATCOM is able to improve the line active power such that active power variations caused by the arc furnace do not propagate throughout the system as shown in Fig. 13. The simulation model and control scheme is described in detail in [28]. The dc capacitor voltages normally vary and are kept in relative balance through redundant state selection [20]. Fig. 16 shows two cycles of the STATCOM multilevel voltage output. The individual module capacitor voltages in each phase for a faulty a phase switch are shown in Fig. 18.

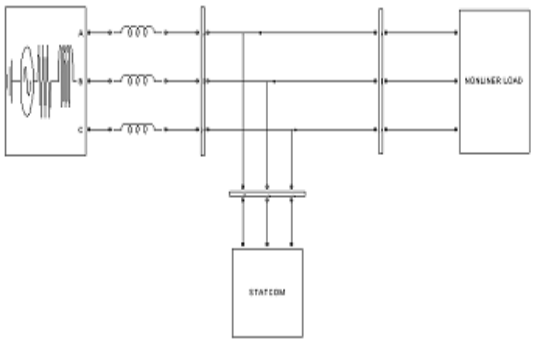

Fig9 Test system

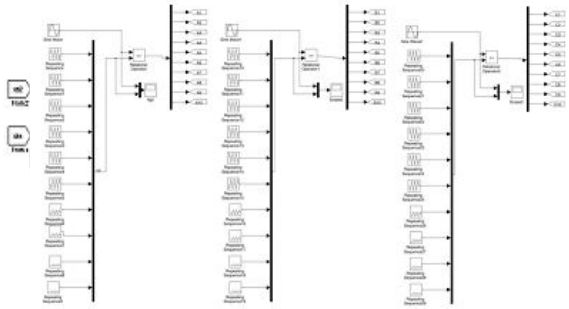

Fig10 phase shift PWM technique

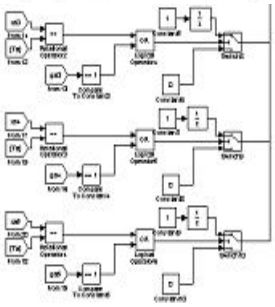

Fig11 Proposed fault detection and remediation control for cell 5.

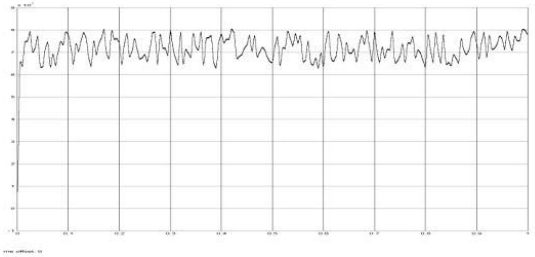

Fig 12. Active power drawn the arc furnace load

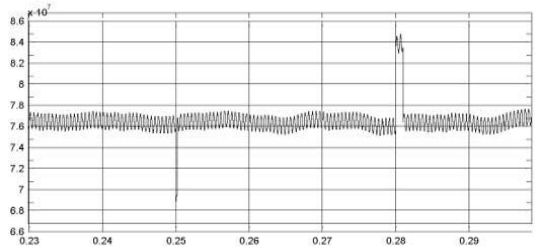

Fig 13 Line active power before, during and after fault

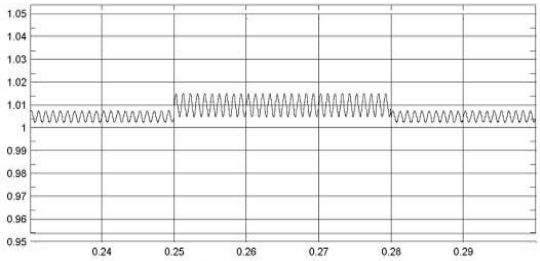

Fig 14. Statcom voltage before, during and after fault

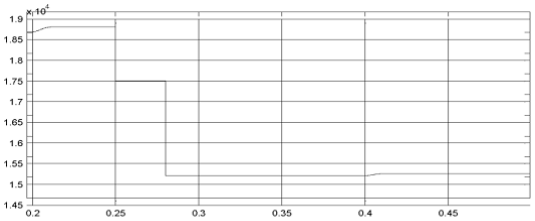

Fig 15. DC voltage before, during and after fault

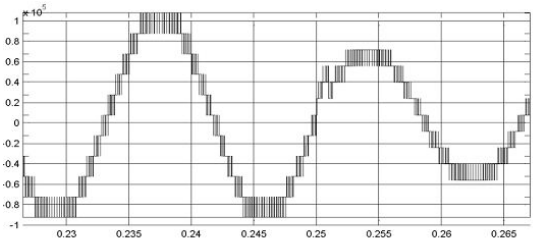

Fig 16 output voltage

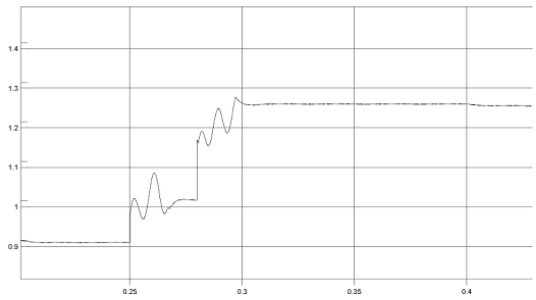

Fig 17. Modulation gain K voltage before, during and after fault

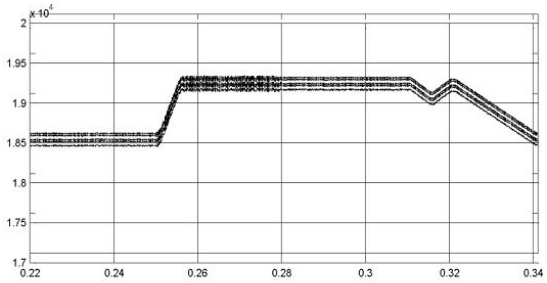

Fig18.Capacitor voltage voltage before, during and after fault

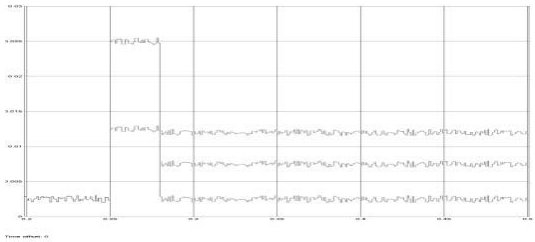

Fig 19 Harmonic content of the faulty cell

V. CONCLUSION

In this paper, a fault detection and mitigation strategy for a multilevel cascaded converter has been proposed. This approach requires no extra sensors and only one additional bypass switch per module per phase. The approach has een validated on a 115-kV system with a STATCOM compensating an electric arc furnace load. This application was chosen since the arc furnace provides a severe application with its non sinusoidal, unbalanced, and randomly fluctuating load. The proposed approach was able to accurately identify and remove the faulted module. In addition, the STATCOM was able to remain in service and continue to provide compensation without exceeding the total harmonic distortion allowances.

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TOWARDS OF SECURED COST-EFFECTIVE MULTI-CLOUD STORAGE IN CLOUD COMPUTING

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Abstract— The end of this decade is marked by a paradigm shift of the industrial information technology towards a subscription based or pay-per-use service business model known as cloud computing. The concept of cloud computing is a very vast concept which is very efficient and effective security services. Cloud data storage redefines the security issues targeted on customer's outsourced data (data that is not stored/retrieved from the costumers own servers). In this work we observed that, from a customer's point of view, relying upon a solo SP for his outsourced data is not very promising. In addition, providing better privacy as well as ensuring data availability can be achieved by dividing the user's data block into data pieces and distributing them among the available SPs in such a way that no less than a threshold number of SPs can take part in successful retrieval of the whole data block. In this paper, we propose a secured cost-effective multi-cloud storage (SCMCS) model in cloud computing which holds an economical distribution of data among the available SPs in the market, to provide customers with data availability as well as secure storage.

Keywords: *Cloud computing, storage, security, cost-effective, cloud service provider, customer.*

1. INTRODUCTION

Cloud computing is simply a rate server. A huge amount of data being retrieved from geographically distributed data sources, and non-localized data-handling requirements, creates such a change in technological as well as business model. One of the prominent services offered in cloud computing is the cloud data storage, in which, subscribers do not have to store their data on their own servers[1], where instead their data will be stored on the cloud service provider's servers. In cloud computing, subscribers have to pay the service providers for this storage service. This service does not only provides flexibility and scalability for the data storage, it also provide customers with the benefit of paying only for the amount of data they need to store for a particular period of time, without any concerns for efficient storage mechanisms and maintainability issues with large amounts of data storage. In addition to these benefits, customers can easily access their data from any geographical region where the Cloud Service Provider's network or Internet can be accessed. An example of the cloud computing is shown in Fig. 1

Since cloud service providers (SP) are separate market entities, data integrity and privacy are the most critical issues that need to be addressed in cloud computing. Even though the cloud service providers have standard regulations and powerful infrastructure to ensure customer's data privacy and provide a better availability, the reports of privacy breach and service outage have been apparent in last few years [4] [3] [6] and [5]. Also the political influence might become an issue with the availability of services [7].

In this work we observed that, from a customer's point of view, relying upon a solo SP for his outsourced data is not very promising. In addition, providing better privacy as well as ensure data availability, can be achieved by dividing the user's data block into data pieces and distributing them among the available SPs in such a way that no less than a threshold number of SPs can take part in successful retrieval of the whole data block.

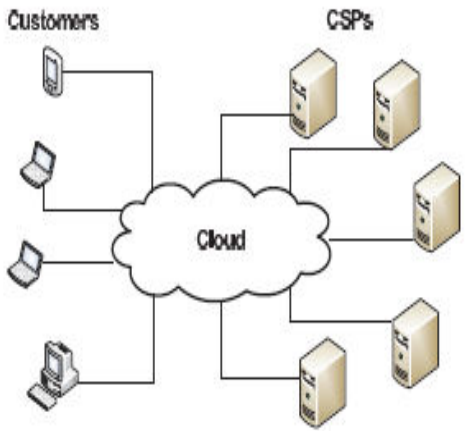

Fig 1. Cloud computing architecture example

Our proposed approach will provide the cloud computing users a decision model, that provides a better security by distributing the data over multiple cloud service providers in such a way that, none of the SP can successfully retrieve meaningful information from the data pieces allocated at their servers. Also, in addition, we provide the user with better assurance of availability of data, by maintaining redundancy in data distribution. In this case, if a service provider suffers service outage [4] [6] or goes bankrupt, the user still can access his data by retrieving it from other service providers.

2. WORKING OF CLOUD COMPUTING

As we have discussed about the basic about the cloud computing in section I, we can say that the cloud computing is a paradigm shift from the distribute computing where an organization uses the resources as services. This is a sort of "utility computing" where you pay-as-you-go like electricity bill. Cloud providers are the companies which manage large datacenters and can expertly manage this datacenters. Cloud users may be a single user or an entire organization which uses services from providers. Cloud users need not to deploy the computing resources at their site. These resources are available at the cloud providers on utility basis and charged on uses basis.

We are taking an example of one cloud service provider that creates the world's largest cloud based infrastructure to understand the working of cloud computing mechanism, that is: **Google.**

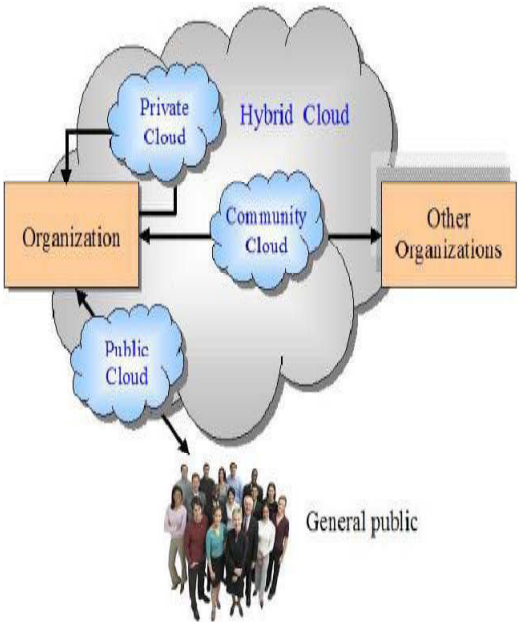

Fig 2. General scenario of traditional cloud provider

Google provides the Google Apps Engine that lets you run web applications on Google's infrastructure. App Engine applications are easy to build, maintain, and scale as your traffic and data storage needs grow. Users just have to create an account in Google and that is the use of Public cloud of Google. User creates his/her own account and mange it, so user establishes his private cloud environment where he can use different services provided by Google. Public cloud is used by the user in his private cloud that creates the Hybrid cloud.

Google Apps now allows free hosting of your e-mail server (with your own domain name), up to 7.3 GB of storage per free user account **(IaaS)**, and free Google Talk, Google Calendar, Google Docs (for creating and sharing documents, spreadsheets and presentations, collaboration in real-time right inside a Web browser window), Google Sites (for easily creating and sharing a group Web site) and Start Page (**SaaS**), and so forth. Google cloud services can be run in any system from anywhere without any consideration of which platform system provide, which OS provide with internet connection. This thing provides the **PaaS** concept of cloud by Google to its user.

3. SINGLE CLOUD SERVICE PROVIDER

Privacy preservation and data integrity are two of the most critical security issues related to user data. In conventional paradigm, the organizations had the physical possession of their data and hence have an ease of implementing better data security policies. But in case of cloud computing, the data is stored on an autonomous business party that provides data storage as a subscription service[8]. The users have to trust the cloud service provider (SP) with security of their data. In, the author discussed the criticality of the privacy issues in cloud computing, and pointed out that obtaining information from a third party is much easier than from the creator himself. Following the pattern of paradigm shift, the security policies also evolved from the conventional cryptographic schemes applied in centralized and distributed data storage, for enabling the data privacy.

3.1. Disadvantage:

- This service does not only provide flexibility and Scalability for the data storage.
- Data losses accrued.
- Do not use cryptography technology so less security
- Need High cost for cloud maintains process

4. MODELS

This section, we will describe our system model and the threat model. This two model goes to explain benefits of cloud storage two multi cloud storage techniques.

A. system overview

We consider the storage services for cloud data storage between two entities, cloud users (U) and cloud service providers (SP). The cloud storage service is generally priced on two factors, how much data is to be stored on the cloud servers and for how long the data is to be stored. In our model, we assume that number cloud service provider for data is to be stored and retrieved, because security is much more higher than cloud service provider.

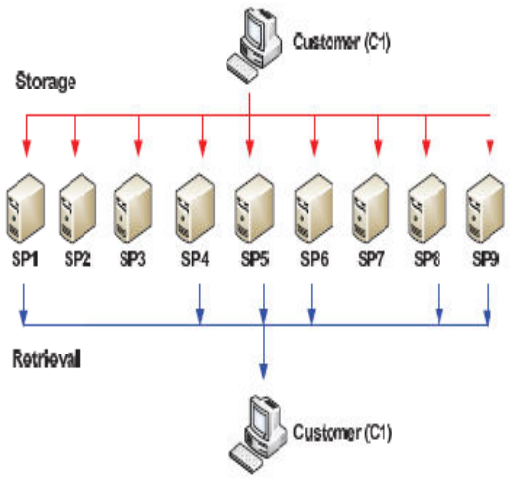

Fig 3. Data Storage and Retrieval

B. Threat model

Customers' stored data at cloud service providers is vulnerable to various threats. In our work, we consider two types of threat models. First is the single point of failure [9], [11], which will affect the data availability, that could occur if a server at the cloud service provider failed or crashed, which makes it harder for the costumer to retrieve his stored data from the server. Availability of data is also an important issue which could be affected, if the cloud service provider (SP) runs out of business. Such worries are no more hypothetical issues, therefore, a cloud service customer can not entirely rely upon a solo cloud service provider to ensure the storage of his vital data.

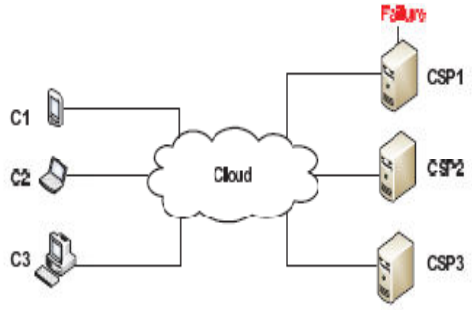

Fig 4. CSP failure

To illustrate this threat we use an example in Fig 4. Let us assume that three customers (C1, C2 and C3) stored their data on three different service providers (CSP1, CSP2 and CSP3) respectively. Each customer can retrieve his own data from the cloud service provider who it has a contract with. If a failure
occur at CSP1, due to internal problem with the server or some issues with the cloud service provider, all C1's data which was stored on CSP1's servers will be lost and cannot be retrieved.

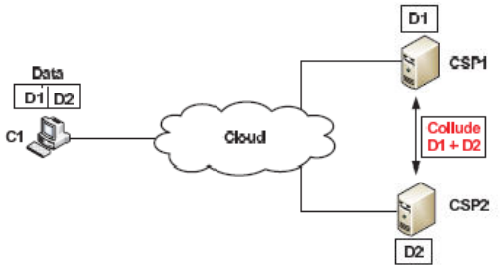

Fig 5. Colluding cloud service providers

We illustrate the colluding service providers' threat in Fig 5. Let us assume that two cloud service providers are available for customer (C1), who want to store his own data securely[8]. In here he will divide his data into two parts (D1 and D2) and distribute these parts on the two available CSPs (CSP1 and CSP2) respectively. The two cloud service providers might collude with each other, and exchange the parts of data that the customer has stored on their server and reconstruct the whole data without being detected by the user.

5. SECURED COST-EFFECTIVE MULTI-CLOUD STORAGE

We proposed an economical distribution of data among the available SPs in the market, to provide customers with data availability as well as secure storage. In our model, the customer divides his data among several SPs available in the market, based on his available budget. Also we provide a decision for the customer, to which SPs he must chose to access data, with respect to data access quality of service offered by the SPs at the location of data retrieval. This not only rules out the possibility of a SP misusing the customers' data, breaching the privacy of data, but can easily ensure the data availability with a better quality of service.

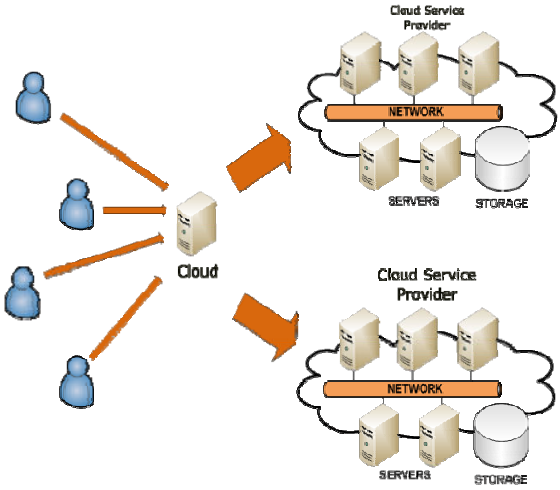

Fig 6. Multi-cloud storage in cloud computing

Our proposed approach will provide the cloud computing users a decision model, that provides a better security by distributing the data over multiple cloud service providers in such a way that, none of the SP can successfully retrieve meaningful information from the data pieces allocated at their servers[7]. Also, in addition, we provide the user with better assurance of availability of data, by maintaining redundancy in data distribution. In this case, if a service provider suffers service outage or goes bankrupt, the user still can access his data by retrieving it from other service providers.

5.1. Advantage:

- Without any concerns for efficient storage mechanisms and maintainability issues with large amounts of data storage.
- Cloud data storage also redefines the security issues targeted on customer's outsourced data.
- Using cryptography technology for data base security
- Less cost and cost based on client requirements.
- Easy to maintains large databases with security
- Avoid database losses.

6. CONCLUSION

In this paper, we proposed a secured cost-effective multi-cloud storage (SCMCS) in cloud computing, which seeks to provide each customer with a better cloud data storage decision, taking into consideration the user budget as well as providing him with the best quality of service (Security and availability of data) offered by available cloud service providers. This work gives a preliminary idea about compare to single cloud storage, security and availability of data is much more efficient in multi-cloud computing. So finally in secured cost-effective multi-cloud storage provide high security compare to other cloud storage.

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ENERGY ACCOUNTING SYSTEM FOR INDIAN ELECTRICITY DISTRIBUTION SECTOR

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Abstract— Energy accounting system (EAS) is required to account the energy flows through various feeders, transformers, substations or various electrical equipment of network systems. Such auditing and accounting shall provide precise accounting of the input and output of energy for any desired time period. The system shall be capable of providing customizable management reports of identifying the gaps in the energy accounted, consumption trend analysis, segregation of technical and commercial losses area/voltage level/ network segment wise for any specified.

Key words- *Energy Accounting & Auditing, EAS Solution, Technical & Commercial.*

I. INTRODUCTION

The aggregated Technical and commercial losses (AT&C) are currently at an unacceptably high level in the Indian Electricity Distribution system and one of the objective of the solution is to provide a detailed area/voltage level/network segment wise energy accounting and auditing to provide a user friendly analysis for efficient monitoring and taking appreciate actions to reduce technical and commercial losses.

I. BUSINESS FEATURES OF EAS SOLUTIOUN

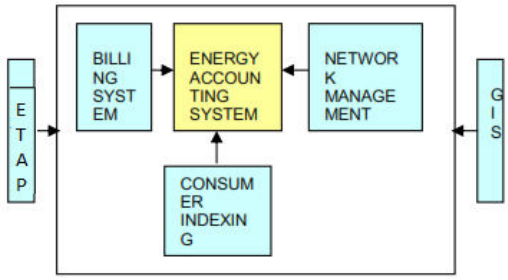


Fig.1 Interfacing Architecture of EAS system

- The system should be primarily being developed for Indian utilities.
- All the functions should be made configurable item to make it suitable from different regulatory requirements across different utilities.
- There should not be any hard coding in the system.
- The system should be easily integrated with the Consumer Indexing System & Network management system.
- The system be should be easily interfaced with the existing Billing system. .
- The system design should such that it can be easily interfaced with external system as discussed under interfaced requirement section of the document.
- The system should functionally meet the Energy Accounting and Auditing requirements of different Indian Utility companies .

II. TECHNICAL FEATURES OF EAS SOLUTION

I. Role of ETAP in Energy Accounting (Fig.2)

The primary objective of the ETAP System is to provide assistance to the Energy Managers in Monitoring & measuring the energy accurately. ETAP system could be utilized for Energy measurement.

The main objectives of the ETAP system are as follows:

- To acquire and monitor the Real time electrical parameters of each energy transaction points for automated Energy Accounting and auditing each feeder, Substations & DT (Distribution Transformers) level.
- Data sharing with the office of CEO, Operation & Maintenance staff for effective monitoring and energy management.
- Information obtained from the substation, feeders & Distribution transformer & consumers.

II. Role of GIS enabled Consumer Indexing & Network mapping:

GIS technology can be effectively used for correct marking of the various Distribution Circles on Geographical area map. GIS mapping of sub-transmission & distribution network from 66kv or, 33kv substations down to LT feeders becomes handy in proper identification, locating and documenting of electrical network assets.

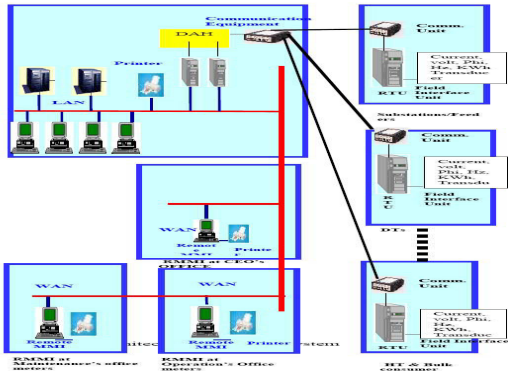
All the existing connections and consumer details can be graphically displayed on the GIS map linked to the database. The mapping of electrical network on GIS base maps and linking with the indexed consumer

database is a multi-step process. The purpose of GIS mapping and indexing of the consumers is to identify and locate all the consumers on geographical map, which are being fed from the Distribution Mains. There may be cases where electric connection exists but it does not exist in the utility's

record it may be a case of unauthorized connection or non –legaderized connection.

On the other hand there may be cases where a connection exist in the utility's record, but it may not exist physically at site.

1. Following reasons could be attributed for such anomalies: The connection might have been disconnected long back but the record may not have been uploaded.
2. It may be a case where the address and other details of the consumers are not correctly recorded



3. The connection might have been disconnected long back but the record may not have been uploaded.
4. It may be a case where the address and other details of the consumers are not correctly recorded

Using GIS, the LT lines coming out from distribution transformer and all service connections from the LT mains can be checked with reference to the consumers connected and accordingly the consumer database can be updated.

Mapping and documentation of electric network, the complete electrical network and network route are digitized and mapped on suitable scale over the base map, using suitable GIS software, so that the change in the network can be timely and correctly updated on a periodic basis. Though software application, queries can be generated to find out the network detail like the make and specification of network elements, the length of feeder and LT conductors, number of transformers of the network.

The network database should have the important details of 66KV/33KV substations, 11KV feeders, DTs and LT lines. Feeder wise and distribution transformer wise consumer segregations to identify the areas of high losses, it is essential to segregate the energy input and feeder wise. The losses are assessed by subtracting the total energy utilization of the consumers from the energy supplied to the respective DT and 11 KV Feeders.using GPS based survey of 11 KV feeders DTs and LT poles, the connected consumers can be identified on the GIS map and segregated distribution transformer-wise and 11KV feeder wise.

iii) role of CIS /energy billing system in EAS(fig.3)

one of the major roles provide by CIS and energy billing system is to provide an account for the 'billed energy' in the specified time period for which the energy accounting activity is being performed. This will be a guiding factor to deduct the commercial loss of the distribution system and thus help in calculating the AT&C loss figure. in the Indian scenario, consumers billing is normally being done on monthly basis and the system keeps record of energy consumption against a consumers. With the adoption of the indexed consumer database, a consumer can easily be mapped with his/her electrical address(substation/HT feeder / DT/ LT feeder / pole etc) and thus the aggregation of the consumption data can easily be performed at any EAS policy level (feeder wise, DT wise etc.) however, an accurate EAS system should take care of the following factors:

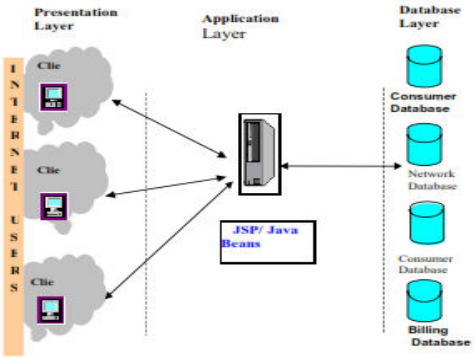


Fig.3 IT Architecture of EAS system

1. Though all the consumers are boiled in a specified billing period (a specific month for the monthly billing scheme),their meter reading data are not same as the reading cycles differs from one group of consumers to other group of consumers. The aggregated consumption figure directly taken from the billing system does not depict the true picture in terms of consumed energy.
2. The billing cycle for the distribution utility may or may not match with the energy accounting cycle.

Both of these factors can be tackled by adopting daily average consumption computation method and multiply the aggregated daily consumption of the group of consumers (under the scope of energy accounting) with the number of days in the energy accounting cycle. Consumption figure for the current month (from CIS /billing system) as well as theHistorical consumption figures (from consumption history data base)are used to calculate the average consumption in daily basis. Different offsetting and prorating algorithm can be use to attain further accuracy.

With the introduction of smart metering system(also gaining popularity in Indian distribution sector) accurate consumption data at a specific interval (half hourly or 15 minutes date) can be obtained and accurate computation of the consumption figure is possible for any accounting period overcoming all the challenges mentioned above.

IV). FUNCTIONAL SPECIFICATION OF EAS SOLUTION.

The solution should adopt statistical process for energy accounting of the electrical network, separate database for assets, location and customer should be one of the features. The energy accounting and auditing solution should be dynamically linked to the customer data base (billing system) through consumer indexing and shall take into account all the chargers in the network and connected customer time to time.

It should be possible to obtain a comprehensive view of the customer via a single data base used to store and access critical account and service data. for the purpose of calculating of ATC(aggregated technical & commercial) losses the changes that take place in the feeding arrangement of the network and connected consumers should be taken into account.

For the purpose of energy accounting relevant metering data of all the incoming and out going feeders from 66KV/33KV substation and distribution transformers has to be available to system.

The figures of import and export of energy though any segment of network during a particular period and figure of energy billed accounted in respect of the connected consumers during the same period will enable calculating AT 7 C loss of the system.

The application shall be such developed that it can be deployed at various administrative and functional offices(e.g. sub division , circle offices etc.) of the utility. It should serve the loss requirements of various levels like substation wise, feeder wise or transformer wise.

The proposed energy accounting system shall contain the following 4 modules:

- utility details
- metering
- meter reading
- network asset details
- network management
- audit and loss analysis

Module 1. Utility details:

This module shall capture all relevant information regarding the utility (including the type of utility) including all the administrative and functional segments. The basic information about the organization, its administrative hierarchy level, geographic spread (e.g. section, subdivision , division etc)shall have available, as also the information regarding functional segment like number of various electrical network under a particular administrative level. This module would also give us the type of power purchase agreements entered into with external utilities.

Process 1.1 utility information:

Process 1.1: entering relevant utility information:

As outlined previously, this process would be responsible for capture of all relevant utility information including basics information like the type of utility, its Geographic's spread, no of sections, divisions, subdivisions. This information is necessary for accurate information with regard energy balance report.

List of input:

Data from utility to be entered in the system organization name, address , mailing, address, contact number, email addressed.

Utility administrative details mentioning the hierarchy level, its name and number.

The function of each administrative segment should be mentioned along with the network hierarchy under this segment.

Process outputs:

Acknowledgement indicating generation of utility code:

Regret message giving reasons existence of utility details, code and administrative and functional segments.

Process 1.2 power exchange point details:

Process 1.2.2: external utility details:

This process captures all the relevant information regarding the external supply feeding point to particular utility network for which the energy accounting and auditing solution will be applied. This should consist of details about the external grid supply point, the external supply agency, the contracted, its details number of incoming feeders,

contract, its details number of incoming feeders,outgoing feeders, their voltage level, grid interconnection points(e.g. for import or export of energy).

List of inputs:
Name, address, company ID of the external grid supply point from where power import/export takes place.
No. of incoming circuits along with voltage level
No of outgoing circuits along with voltage level
The contractual capacity
The validity and type of contract.

List of outputs:
Acknowledgement indicating generation of external utility code, regret letter giving reasons-like non existence of company exchange point details.

Module2: metering

process 2.1: meter movement
meters delivered at stores are subject to acceptance test and upon clearance are entered in the meter database. All on site and off site tests conducted the meter are to be recorded from the meter test reports there from the body of the equipment to be audited is to be recorded from the meter sealing certificates.

List of inputs:

Cost of meter from PO
From manufacturer test certificate-
10 digit meter serial number
Purchase order number
Manufacturer ;s name
Category-direct, CT operated, CT/PT operated
TVM/non TVM
Meter specification-single/poly phase; capacity and accuracy class.
Type-electronic/electromechanical
Date of delivery at stores from the challan
From the sealing certificate-

Date of installation/removal, consumer number,bill number, multiply factor, dial factor, CT/PT serial number and ratios, reason(and sub reason) for installation (new connection /load change/replacement with defective or burnt meter or other).removal- PD/load enhancement/ defective/burnt or others.

Opening /closing reading (kwh, kvarh, max demand, TOD registers)

From the meter test reports date of testing,% error , readings at the time of testing and meter testing personnel code.

Process outputs:

Update meter database
Update application database
Report on meter installations for each reasons-
Meter no. equipment date of installation, reason
report on meter removals for each reason-meter
No. equipment, date of removal, reasons
Meter history
Report on meter testing-meter no. date of testing, meter make , percentage error, accuracy class installation details-equipment and location
For all cases in a given period
For cases exceeding permissible limits in a given period.
Vendor wise meter failure report- meter no. make, PO no., failure reason, period of service
(date of removal –date of delivery)
Inventory report for determining numbers of meters in circuits and off circuits-meter type, total number of in –circuit meters, off circuit meters, scrap
Scrap value based on depreciation percentage given by the user.
Schedule for meter testing for a give period-meter no. equipment, last testing date ,% error from meter database
Name address and load from consumers database consumption pattern for last 3 billing periods(configurable in system)from the billing database.

Process 2.2: meter replacement:
Any replacement of meter arising due to changes in load, defective meters/burnt metes shall be accompanied with date of replacement, closing and opening readings, MF ,dial factors and other sealing detail in the sealing certificate. Entry screen should be available in the meter movement module(installation details).in case of burnt or sluggish meters, a provision for debit adjustment for next audit metering cycle may be made for sluggish or burnt meters.
List of inputs:
Data from movement model closing reading and date of old meter and opening reading date and MF of new meter.
Debit adjustment for sluggish or burnt meters.
Process outputs:
Update meter change details in meter data Update debit adjustment for next meter reading period.
Module3: Meter reading
Basis system feature for obtaining meter reading would include:
Interface capability with ETAP/Meter Reading Instrument (MRI) data for uploading meter readings.
Interface capability with Automatic Meter Readings (AMR) readings.

Capability of capturing meter reading data from a Meter Reading Book in case of manual reading system.

Ability to cater to change in the metering cycle. Metering in certain case may be hourly,daily,fortnightly etc.

Process 3.1: Maintain Reading Schedule

The system generates a meter reading itinerary at for all location where audit meters are installed using the number of meter readers available and the Audit equipment where the meter reading are to be taken. The frequency of these itineraries can be weekly, fortnightly or monthly. After itinerary generation, it is sent to the department, which may be expected to manage these readings.

Process output:

Location specific reading itinerary

Dispatching the above to the local SBU Unit of the concerned department.

Process 3.2 Capture and validate Meter reading

Depending upon different mode of meter reading as described above, the system should be able to capture and store the readings to populate the reading data store of the application. For ETAP or MRI interface the application will flat file inputs in a pre definedformat.For manual the entry screen is provided to capture manual readings. After reading data is captured the system should generate an Exception report highlighting possible inconsistencies in the metering data.

List of inputs:

Group wise reading for current month in a flat file or manual entry of meter reading having Equipment ID, present readings, reading dates, remarks and meter reader code. Average consumption per day of last 3 Audit cycle with firm readings. Range of permissible variation for generating exception list.

Process outputs:

Exception list for variation in consumption list of cases with remarks meter mismatch. Not Read because meter Mismatch, not read because meter not traceable, Meter not accessible meter faulty. Group wise meter reader wise performance report-Total meters to be read, No of reported meter mismatches meter faulty.

Module 4: Network Asset Details

The module details with the details of each and individual asset available within the Utility power network. This includes Power transformer,isolator, metering device and pole details.

This network assets considered under the scope of this application are: Substation, Transformers, cables ,Poles/pillars. Nameplate details as well as other relevant technical parameters(such as resistance ,reactance of cables)of these assets are capture under this module.

Process 4.1 Updation of Network Asset Details

This sub module deals with the updation of assets in the transmission and distribution network of the utility including details of substations, Transformers(both power and distribution),Breaker, Feeders, Poles/Feeder Pillars.

List of inputs:

Details about HT Substation like name of HT substation, location of HT substation, capacity of each substation number of power transformer under a particular HT substation, no of feeders. Details about Distribution transformer and Feeders and electric poles.

Process Outputs:

Acknowledgement of data entered into the system through generation of unique code.
Details of substation .
Details of Transformer.
Details of Feeders.
Details of Poles/Feeder pillars.

Module 5: Network Management

This module deals with the mapping of Electrical Assets in the electrical network of the utility. In other words the scope of this module includes mapping the poles to the Distribution transformer,

The distribution transformer onto the HT feeder and feeder onto the Distribution station and finally onto the substation of the transmission Network Process 5.1:Asset Mapping

The asset to be mapped is first selected and then asset to which the previous assets is to be mapped is selected.

List of inputs:

Equipment type, as to whether it is a Transformer, Substation, Process output:

Location specific reading itinerary

Dispatching the above to the local SBU Unit of the concerned department.

Process 3.2 Capture and validate Meter reading

Depending upon different mode of meter reading as described above, the system should be able to capture and store the readings to populate the reading data store of the application. For ETAP or MRI interface the application will flat file inputs in a pre definedformat.For manual the entry screen is provided to capture manual readings. After reading data is captured the system should generate an Exception report highlighting possible inconsistencies in the metering data.

List of inputs:

Group wise reading for current month in a flat file or manual entry of meter reading having Equipment ID, present readings, reading dates, remarks and meter reader code. Average consumption per day of last 3 Audit cycle with firm readings. Range of permissible variation for generating exception list.

Process outputs:

Exception list for variation in consumption list of cases with remarks meter mismatch. Not Read because meter Mismatch, not read because meter not traceable, Meter not accessible meter faulty. Group wise meter reader wise performance report-Total meters to be read, No of reported meter mismatches meter faulty.

.The equipment location. Voltage level of the equipment from the voltage level. The asset to which this equipment is to be mapped into process output.
The selected asset mapping details.
The asset mapping theory.
Module 6: Audit And Loss Analysis
Functionality under this module include the total audit and loss trend analysis of utility network for a specified time period. The audit and loss analysis may be applied to any network or to a particular administrative segment of the utility. It should be able to compute aggregate technical and commercial loss(as defined by regulatory).It should be able to estimate the consumption profile of each network segment of the utility and provide an insight into the losses. This system shall be capable of providing customized management report, Process output:
Location specific reading itinerary
Dispatching the above to the local SBU Unit of the concerned department.
Process 3.2 Capture and validate Meter reading
Depending upon different mode of meter reading as described above, the system should be able to capture and store the readings to populate the reading data store of the application. For ETAP or MRI interface the application will flat file inputs in a pre defined format.For manual the entry screen is provided to capture manual readings. After reading data is captured the system should generate an Exception report highlighting possible inconsistencies in the metering data.
List of inputs:
Group wise reading for current month in a flat file or manual entry of meter reading having Equipment ID, present readings, reading dates, remarks and meter reader code. Average consumption per day of last 3 Audit cycle with firm readings. Range of permissible variation for generating exception list.
Process outputs:
Exception list for variation in consumption list of cases with remarks meter mismatch. Not Read because meter Mismatch, not read because meter not traceable, Meter not accessible meter faulty. Group wise meter reader wise performance report-Total meters to be read, No of reported meter mismatches meter faulty.
gap's in the energy accounted.
Process 6.1 Loss Analysis
The process deals with the depiction of the technical commercial, and the total loss for a specified period of times.
List of inputs:
Equipment Id, Administrative level, voltage level. Audit cycle: Process Output Technical loss for the audited area, equipment for the above cycle Commercial loss in MU or percent. Aggregate Technical And Commercial (ACT)loss.
Process 6.2: Audit Result Reporting and trending
This process takes care of customized management report with regard to technical,commercialand total losses for an audit location/asset for a particular period. The system should also cater for trending of the losses/energy consumed over a period of time as may be specified by the user.
List of input:
Audit device/Audit location
Report choice-Energy consumed or loss Specified time period
Loss category -Commercial,Technical.
Process Output:
Loss analysis report location/voltage/equipment wise for a particular .Energy consumption report location/voltage/equipment wise for a particular period.Loss and Energy Consumption trends.

CONCLUSION:

With the help of energy accounting system following report can be generated in regular interval for better energy monitoring and management:
Area wise/voltage wise/feeder wise/DT wise technical and technical loss
Consumption trend of different consumer Base along with their consumption pattern
Details in input and output of energy of
Substation , feeder and distribution transformer

Finally identification of potential energy losses Area both technical as well as commercial.

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MODELING & SIMULATION OF PRIMARY-SIDE-CONVERTER-ASSISTED SOFT-SWITCHING SCHEME FOR AN AC/AC CONVERTER IN A CYCLOCONVERTER-TYPE HIGH-FREQUENCY-LINK INVERTER

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Abstract:- The Emerging trends of high-power-density power electronics interfaces for renewable- and alternative-energy sources have led to the need for high-frequency-inverter designs without compromising energy-conversion efficiency. In that context, a zero-voltage-switching (ZVS)-based scheme is described in this letter, for a cycloconverter-type high-frequency-link inverter, which is applicable for renewable- and alternative-energy sources as well as other commercial applications. The roposed
scheme achieves the primary-side-converter-assisted switching of the ac/ac converter switches under ZVS condition. The modes of operation of the ac/ac converter are explained to outline the behavioral response.

Index Terms— *Zero voltage switching (ZVS), ac/ac converter, inverter, cycloconverter, renewable, alternative, energy sources, photovoltaic, fuel cell, high frequency, high-frequency link*

I.INTRODUCTION

High efficiency, low cost, and high power density are important attributes of inverters for applications, including distributed-generation systems with renewable- and alternative-energy sources (e.g., photovoltaic, wind, and fuel cells), energy-storage systems, vehicle-to-grid applications, electric/hybrid-electric/fuel-cell vehicles, compact power conversion modules for naval, space, and aerospace applications, and battery-based uninterruptible power supplies. In such systems, galvanic isolation is often required for safety concerns and voltage and current scalabilities. In that regard, a high frequency-transformer-based approach can be a preferable choice from the standpoint of weight, footprint, and cost reduction. Among the possible topologies, a high-frequency-link (HFL) pulsewidth modulated (PWM) inverter can eliminate the intermediate LC filter that is needed for a conventional high-frequency (HF) fixed-dc-link converter approach. Furthermore, as compared to a resonant-link inverter, an HFL inverter yields lower switch stress, better total harmonic distortion (THD), and simpler all-device structure(i.e., no passive components within the power stages). Thus, the PWM HFL inverter approach is better suited from the viewpoints of cost, efficiency, and portability. Two typical HFL inverter topologies have been proposed in the literature. One is a rectifier-type HFL (RHFL) inverter. It comprises a primary-side HF dc/ac converter feeding an HF transformer, which is followed by an ac/dc converter and a pulsating-dc/ac converter. Thus, the RHFL inverter topology possesses a structure similar to that of a conventional fixed-dc link inverter except for the absence of the dc-link filter. One of the features of the RHFL inverter topology is that the input signal to the output ac/ac stage is pulsating dc in nature (with encoded information of the primary-side HF dc/ac converter) that can be used to modulate the ac/ac stage with reduced switching loss. The other class of topology is a cycloconverter-type HFL (CHFL) inverter, as illustrated in Fig. 1, which reduces the conversion complexity by directly placing an ac/ac converter to the secondary side of an HF transformer, which is fed by a primary-side HF dc/ac converter. In the CHFL topology, because the output stage is a single stage, the input to the ac/ac converter is an HF bipolar ac signal generated by the primary side dc/ac converter. Therefore, switching the ac/ac converter using this primary-side converter information for switching loss reduction is a possibility. One such zero-voltage-switching (ZVS) mechanism, leading to reduced-loss switching with the assistance of a primary-side dc/ac converter, is outlined next in this letter which can be extended to a higher number of phases following the same principle. The results on the efficacy of the ZVS-based inverter and its performance show satisfactory performances. A new ZVS scheme for the ac/ac converter of a CHFL inverter has been outlined in this letter. By mitigating the device switching loss, the ZVS scheme enables one to potentially choose power MOSFETs with lower ON-state resistance at the price of slightly higher output capacitance. Diode and an active device (e.g., MOSFET or IGBT) conduct during the transition and the ON-states, in the ZVS scheme, the diode only plays a small role during the transition. As such, the reverse recovery of the diode during the transition is reduced. These loss-mitigating mechanisms yield an improvement in the inverter (i.e., dc/ac converter followed by the ac/ac converter) efficiency of over 2% at the rated power and over 3% at around 20% of the rated power using the ZVS scheme. Aside from demonstrating the inverter efficiency using the ZVS scheme, we have also demonstrated the output-voltage yield and THD. They clearly show that a higher voltage and slightly better THD are yielded using the ZVS scheme due to higher efficiency and soft switching transition.

II MODELING OF CASE STUDY PRINCIPLE OF THE ZVS SCHEME

With reference to the CHFL inverter illustrated in Fig. 1, Figs. 2 and 3 show two switching schemes (for the ac/ac converter) that will be referred to as the "conventional scheme" and the new "ZVS scheme." The operation of the HF full bridge dc/ac converter (which remains the same for

both the schemes), along with the operation of the conventional scheme. The dc/ac converter produces an HF bipolar voltage (Vsec) across the transformer using sinusoidal pulse width modulation. Bipolar voltage is required per switching cycle to ensure transformer flux balance. For the conventional scheme and as illustrated in Fig. 2, the ac/ac converter has two operating scenarios: one with the polarities of the output voltage and output current being the same and the other with the polarities of the output voltage and output current being opposite. For the first scenario, the ac/ac converter switches operate at line frequency with the anti-parallel diodes switching at HF in Fig. 3 in which the diodes turn off). For the second scenario, the half-bridge ac/ac-converter switches operate at HF in Fig. 3 yielding higher switching loss. For the ZVS scheme, the operating modes (for positive inverter output current and voltage, Vsec ≥ 0, and Vsec ≤ 0) of the ac/ac converter are, along with the switching sequences, which are shown in Fig. 3. The primary side dc/ac converter dynamics is not illustrated. However, the voltage across the transformer secondary (Vsec = 0or Vsec> 0) demonstrates that the primary-side dc/ac converter is operating in either the zero state or the active state. It is also noted that, even though the output of the dc/ac converter is bipolar, the principle of operation of the ZVS scheme does not change for negative primary-side voltage output. The operating modes are discussed below

Mode 1: In this mode, Vsec = 0. All of the ac/ac-converter switches are turned on. As such, the output current is shared equally between the two arms of the half-bridgeac/ac converter. Note that the current sharing between the two arms results in lower conduction loss.

Mode 2: This is a zero-state interval during which Vsec = 0. At the beginning of Mode 2, the switch S3 is turned off under ZVS condition. Half of the output current that was flowing through the lower arm now begins to transfer to the upper arm. Eventually, the switches S1 and S2 carry the output current.

Mode 3: This mode initiates when Vsec rises from zero voltage to the dc-bus level and ends with switch S3 blocking Vsec.

Mode 4: In this mode, switches S1 and S2 support the output current. Because switch S3 blocks Vsec, switch S4 can remain on, or it can be turned off under zero-current condition.

Mode 5: This mode initiates when the primary-side dc/ac converter attains a zero state, and as such, Vsec approaches zero voltage. The output current is primarily supported by switches S1 and S2 while the output capacitance of switch S3 discharges, and eventually, it is clamped by the antiparallel diode of S3.

Mode 6: Similar to Mode 1, this is a zero-state interval. This mode ends when switch S3 turns on under ZVS condition. Subsequently, the output current is shared between the two arms of the ac/ac converter. At the end of this mode, a half switching cycle is achieved. The other six modes (Modes 7–12) corresponding to positive output current and output voltage and Vsec ≤ 0 can be explained following the explanations for Modes 1–6.

III. MATLAB DESIGN OF CASE STUDY

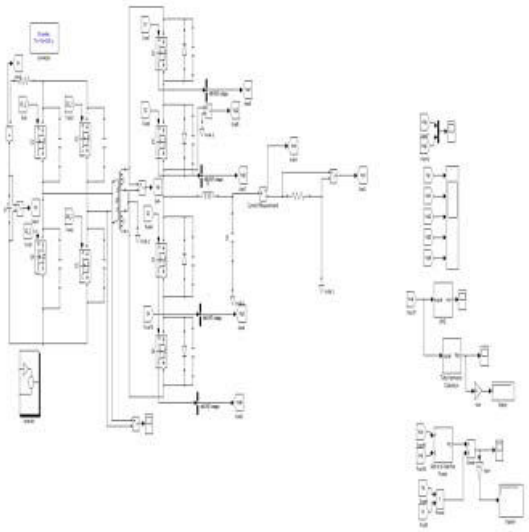

Fig:-1 CHFL Inverter Comprising A Dc /Ac and an Ac / Ac Converter primary and Secondary sides of the transformer

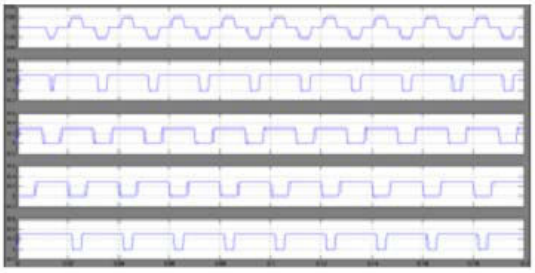

Fig:-2 gating signals of the ac/ac converter for the „zvs „scheme when the bipolar transformer secondary voltage is positive /negative

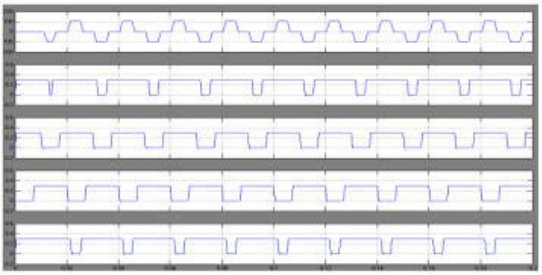

Fig:-3.gating signals of the ac/ac converter for the „conventional scheme „when the polarities of the output voltage and current are the same and opposite

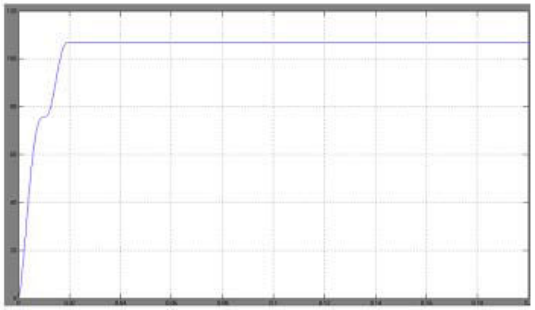

Fig:-4.output power and efficiency of the zvs scheme

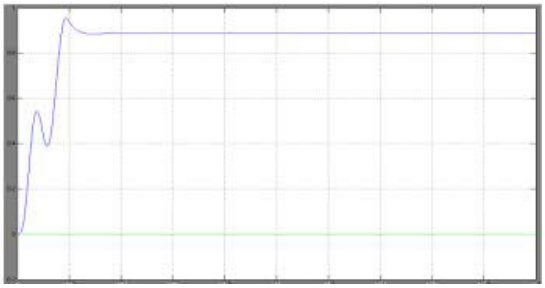

Fig:-5..output power and efficiency of the Conventional scheme

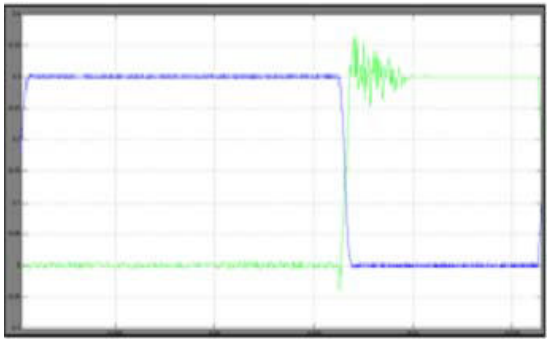

Fig:-6.Mosfet(falling trace)drain to source voltage and (rising trace)gate to source voltage for „zvs" scheme

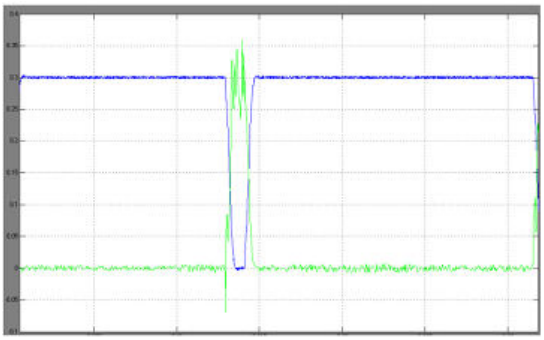

Fig:-7..Mosfet(falling trace)drain to source voltage and (rising trace)gate to source voltage for „conventional"

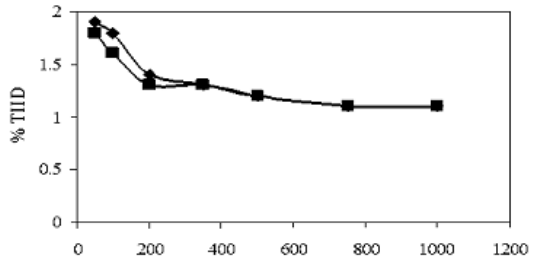

Fig:-8.. Experimental THD of the inverter output voltage using the ZVS and the conventional schemes (bottom and top traces, respectively)"

IV. RESULTS

The efficacy of the ZVS scheme is ascertained using openloop control experiments on the CHFL inverter topology(shown in Fig. 1). The results of the ZVS scheme are alsocompared with the conventional scheme for the ac/ac converter. The dc/ac converter operates at 20 kHz whichtransforms to a 40 kHz PWM frequency at the output of thesecondary-side ac/ac converter due to frequency doubling.The rated power of the inverter is 1 kW while the input voltage is set at 36 V. For the dc/ac converter, OptiMOS power MOSFETs (IPP08CN10N G) from Infineon are used, which have with following key specifications: voltage and current ratings - 100 V, 95 A, gate charge - 100 nC, on-state resistance - 8.2 mΩ. For the ac/ac converter, Q-class HiPerFET power MOSFETs (IXFX21N100Q) from IXYS are used. The key specifications of this device are as follows: voltage and current ratings - 1000 V and 21 A, gate-to-source and gate-todrain stored charges – 27 and 18 nC, on-state resistance - 0.5 Ω. A nanocrystalline core (STX 1060M1) is used for the center-tapped HF transformer with number of primary and secondary turns as 12 and 104(i.e. 2 x 52), respectively. Values of the output filter inductance (Lf) and capacitance (Cf) are set to be 2.4 mH and 0.5 μF, respectively. Figs. 4,5shows the comparison of the inverter efficiencies obtained using the ZVS and the conventional schemes. Inverter efficiency using the ZVS scheme shows an improvement of over 2% at rated power and over 3% at around 20% of the rated power. Figs. 6 and 7 show the overlapping gate-to-source and drain-to-source voltages for the conventional and ZVS schemes, illustrating a softer discharge mechanism for the ZVS scheme. The results of the open loop inverter clearly show higher output-voltage yield for the ZVS scheme as compared to the conventional scheme due enhanced efficiency obtained using the former. Finally, Fig. 8 compares the total harmonic distortion (THD) of the inverter output voltage using the ZVS and the conventional schemes. The conventional scheme results in a small kink near the zero crossing. Hence, as the output power reduces and the switching effect becomes more dominant, the slight difference shows up as a small difference in the THD. However, at higher power, when the peak current is higher, the difference is negligible.

V. SUMMARY & CONCLUSION

A new ZVS scheme for the ac/ac converter of a CHFL inverter has been outlined in this letter. By mitigating the device switching loss, the ZVS scheme enables one to potentially choose power MOSFETs with lower ON-state resistance at the price of slightly higher output capacitance. Unlike the schemes outlined in [17]–[20], where a diode and an active device (e.g., MOSFET or IGBT) conduct uring the transition and the ON-states, in the ZVS scheme, he diode only plays a small role during the transition. As such, the reverse recovery of the diode during the transition is reduced. These loss-mitigating mechanisms yield an improvement in the inverter (i.e., dc/ac converter followed by the ac/ac converter) efficiency of over 2% at the rated power and over 3% at around 20% of the rated power using the ZVS scheme. Aside from demonstrating the inverter efficiency using the ZVS scheme, we have also demonstrated the output-voltage yield and THD. They clearly show that a higher voltage and slightly better THD are yielded using the ZVS scheme due to higher efficiency and soft switching transition.

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AN ENHANCED EDIFICATION FOR VALIDATION OF FACTUAL REQUIREMENTS

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Abstract---Aspect oriented paradigm builds on the concept of separation of cross cutting concerns. The systematic activities of Separation of Concerns (SoC) are - identification of concerns, separation of concerns, representation of concerns, and composition of concerns. Few Aspect Oriented Requirement Engineering (AORE) models provide validation of elicited aspects by walkthroughs, inspections, or formalized procedures. In this paper, we have extended an already proposed edification to provide two levels of validation, which validates correct elicitation of concerns (aspect) from requirements. The proposed model validates the elicited aspects by graph validation.

1. INTRODUCTION

Aspect Oriented Software Development (AOSD) separates crosscutting concerns to avoid tangling and scattering of requirements, design or code at the various stages of software development lifecycle. The crosscutting concerns are modularized to independent modules called aspects. Crosscutting concerns can be identified at any stage of software development life cycle, i.e., requirements phase, design phase, and implementation phase. Identification of aspects at requirements phase, helps in identifying, separating, and isolating the concerns at the earlier stage. Thus the tangling and scattering is not propagated to the next stage of development phase. More emphasis is laid on dentifying concerns at the requirements stage as it reduces the cost of implementation, maintenance, and increases evolvability . The aspect oriented requirement models are
based on the requirement engineering approaches - viewpoint oriented approaches, use case /scenario oriented approaches, goal oriented approaches and other approaches [2]. These models elicit concerns on the basis of the four
activities of separation of concerns: identification of concerns, separation of concerns, representation of concerns, and composition of concerns [3][4][5]. To achieve well-defined document containing the user requirements that satisfies these prerequisites, The proposed edification [1] provides refinement and verification of aspectual requirements. In this paper, we have extended the edification to provide two levels of validation. The second level of validation technique is incorporated to generate graphs for the concerns (in this paper we are treating concerns as aspects) elicited from the three models. The three graphs viewpoint graph, goal graph, and use case graph are merged together according to the weave table criteria, which leads to generation of aspectual graph. The complete validation technique has been discussed in section 3, along with the edification . In section 2, the related work has been discussed. Section 4 concludes the paper.

2. RELATED WORK

There are few Aspect Oriented Requirements Engineering (AORE) models, which validate the correct elicitation of aspects. Few of the AORE models such as Theme [16], goal oriented model proposed by Yu et al. [20], and domain analysis and engineering AORE model proposed by Kuloor and Eberlein [21] provide validation of elicited aspects by back tracking from design to requirements phase, by formal analysis approach, and by walkthroughs, respectively. The AORE models are based on viewpoint oriented approaches, use case based approaches, the non-traditional requirements engineering approaches for elicitation of requirements from
early phase, i.e., requirements phases. Most of these AORE models identify concerns, separate the crosscutting concerns, resolve conflicts, and weave them to give a picture of complete system. Some of the characteristics that each AORE models are may have are, support for evolvability requirements, traceability from design to requirements, verification and validation of elicited aspects, and other characteristics.. The AORE model based on goal oriented requirement engineering approach identifies concerns of systems on basis of functionality or goals. Maria et al. [3] proposed a Goal oriented Requirement Methodology based on the principles of Separation of Concerns (GREMSoC). This methodology provides reuse of
use-cases, refinement of soft goals by operationalization and enhances modularity. Composition rules enable to identify where toapply the non-functional requirements in a usecase. GREMSoC does not provide detailed methodology to emove conflicts. Araujo et al. [6] proposed a use-case based requirement approach, which identifies concerns from different usage/scenarios of system. It is a template based approach for identifying aspectual use-cases which are modeled, providing traceability similar to GERMSoC. There are many proposed approaches for identifying aspect by use-case requirement engineering methodology [7][8][9]. The

AORE model proposed by Rashid et al. [11] is an extension! enhancement of [10]. This model applies viewpoint oriented approach, which identifies stakeholders' requirements. This approach identifies and specifies concerns by viewpoints and XML. Arauijo et al. [11] proposed a edification based on viewpoint requirement engineering approach. It also generates templates, which explicitly identify crosscutting non functional requirements. Jackson [12] proposed a problem frame requirement methodology that extracts aspects from the problem domain rather than the solution domain, by disintegrating problems into sub-problems and defining composition rules to resolve conflict and ambiguities. Grundy [14] proposed an AORE model based on the component requirement engineering approach. There have been many models (Cosmos [17][18] and CORE [15]) proposed for the concern oriented or multidimensional separation of concern approach. Moreira [15] proposed Concern Oriented Requirement Engineering (CORE) a concern oriented approach that is an extension of [11]. It introduced projection table, which reduced the concern dimension. Theme [16][19] is an AORE model that is not based on conventional approaches viewpoint, use case/ scenario and goal oriented approach. Theme extracts crosscutting concerns by keyword and lexical analysis.

3. PROPOSED EDIFICATION

The proposed edification enhances the validation methodology presented in [1], which amalgamates three Aspect Oriented Requirement Engineering (AORE) approaches: viewpoint oriented approach, goal oriented approach, and use case approach. Our proposed edification
provides second level of validation by introducing graph validation phase.

A. XML Validation Phase

For clarification and better understanding the XML validation phase proposed in [1] has been explained to associate it with the current proposed methodology:

The concerns are identified from the viewpoint oriented approach, use case approach, and goal oriented approach. These concerns are specified in XML format. This leads to generation of XML files for each approach. The duplicate concern remover (DCR) receives the three XML files generated from previous modules. These three files are compared to construct a common XML file. Three files are compared with each other to remove redundancy by checking the number of requirements associated with the identified concerns and if the three XML files have similar requirements they are merged to generate a single XML file. If DCR is unable to merge the files, then these are given as input to Refinement and Verification Module (RVM). RVM applies set of heuristic rules to resolve conflicts between the concerns and generate single XML file for each concern. Finally the aspect generator module receives the XML files
from RVM and converts them into an aspect.

B. Graph Validation Phase

The enhanced level of validation introduced to [1] is graph validation phase. The graph validation approach is based on the similar idea of XML validation phase, for each requirement engineering approach a graph is generated. These graphs are compared and merged to a single graph by applying heuristic rules to partially validate the aspects. The merged graph is converted to XML files. The detailed procedures are as follows:

Step 1: Graph Generation. For each of the requirement engineering approaches in [1] graphs are generated. The first graph generated is viewpoint graph, which is generated from perspective of each viewpoint. The aspects associated with particular viewpoint are knitted together. The second graph generated for the requirement engineering approach is goal graph. The aspects are associated with each goal. In order to reduce the graph complexity, the graphs are considered from the perspective of a viewpoint (details in [13]). Third type of graph is use case graph. This graph incorporates different aspects, which are identified from use-case based aspect oriented requirement engineering approach.

Step 2: Graph weaver. The graph weaver receives the three graphs (viewpoint graph, use case graph, and goal graph) as input. In order to validate the correct elicitation of aspects, we merge the viewpoint graphs, goal graph, and use case graph on the criteria defined by a weaving table. Weaving table contains all rules and heuristics that define how to merge the three graphs that are generated from three different requirements engineering approaches.

Step 3: Duplicate Node Remover. The duplicate node remover (DNR) receives an extremely cluttered and complex merged graph. In order to reduce the complexity and redundancy, manual analysis is performed to identify aspects impacting same non-functional requirements. This merged graph has duplicate nodes as well as conflicting nodes. In this step, only duplicate nodes are removed from the graph. However, if the number of non-functional requirements, which are being spanned by an aspect, vary then the aspect is moved to conflict resolver.

Step 4: Conflict Resolver. The conflict resolver receives the graph having redundant aspects, which can not be merged together due to varying number of non-functional requirements. All the conflicts due to varying number of non-functional requirements within each aspect are removed by this component.

Once all duplicate nodes are removed and conflicts have been resolved, the reduced graph is termed as aspectual graph. This graph becomes input to the Aspectual Graph Parser.

Step 5: Aspectual Graph Parser. This component receives aspectual graph as input and converts the aspects and associated requirements into XML file. This file is then used to compare the converted XML file and the XML file generated from XML validate phase.

C. Aspect Validation

In this step, the aspectual graph and the output generated by aspect generator, which is in XML file format are compared to validate the complete coverage of the requirements, i.e., how many non-functional requirements are being impacted by an aspect. Also validating the aspects identified and the requirements associated with aspects are correctly elicited.

Thus the model converts the identified concerns / aspects from each AORE model to their respective graphs - viewpoint oriented approach generates viewpoint graph, the goal oriented approach generates goal graph, and use case oriented approach generates a use case graph. These three graphs are merged into one graph, which leads to duplicate concern !aspect node. The duplicate nodes are discarded after manual analysis. This process' output leads to an aspectual graph that is provided as input to aspectual graph parser. The graph parser generates an XML file for the aspectual graph. In parallel, the XML files are produced from each of the AORE model and this leads to duplicate concerns. After scrutinizing the XML file to remove duplicate concerns and ambiguities the final XML file is compared with the Aspectual graph. This comparison validates that the identified aspects are correctly elicited from the initial requirements gathered.

4. CONCLUSION

In this paper, we have introduced another level of validation to an already proposed edification . The extended methodology introduces graph validation phase .Since most serious problems associated with software development are related to validation phase. For concerns elicited by the viewpoint oriented approach, use case based approach, and goal oriented approach, graphs are created. The three graphs are merged to analyze coverage of all the requirements that are being impacted by an aspect. The inconsistencies and redundancies are removed from the merged graph to generate an aspectual graph. From aspectual graph XML file is generated that is compared with the ouLtpUt of previous edification to validate the correct elicitation of aspects from the requirements.

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REVIEW ON REALIZATION OF INTELLIGENCE MONITORING SYSTEM BASED ON REMOTE SENSOR TECHNOLOGY

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Abstract:-The objective of our project is to design and implement intelligence monitoring system through sensor technology which will help against theft or unauthorized person identification. In our project we have used RF technology for data transfer between transmitter and receiver side. RF Transmitter has Microcontroller which lead to control transmitter section modules like magnetic and PIR motion sensor included in our project. The monitoring will be noted by GSM and LCD which is placed in our receiver side. Theft occurrence can be noted by the magnetic and PIR motion sensor by which the magnetic sensor is attached to the doors and the motion sensor senses the human movement inside the secured area. This can be done in our project by using multichannel ADC. RF receiver section contains the GSM modem, LCD display, and alarm. The RF transmitter and receiver which operate at 433MHz can be able to transmit and receive the data effectively at a low cost. The purpose of LCD is to display the theft occurrence.

Keywords: *Home network,embedded c,GSM,sms,remote controlling,GPRS modem,Rf technology,RF receiver*

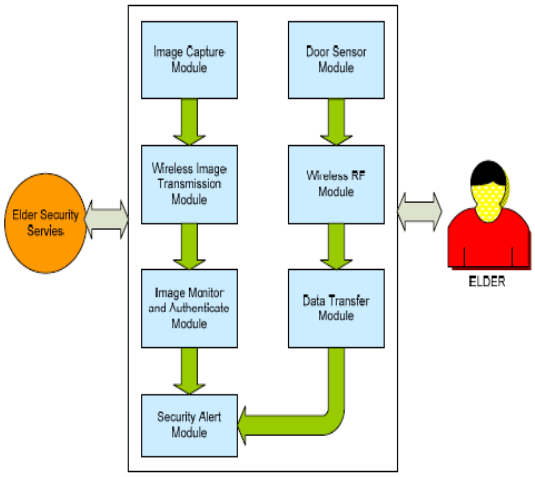


Figure 1. IWHSS System Overview

A. Person Identification Function (PIDF):

Usually the main door of the house consists of a calling bell. But an elder may be inside his/her room, who has to walk all the way to the entrance or use their wheel chair to go to the entrance to open the door. Most of the time, it would be very inconvenient for the elders. IWHSS provides an easy solution for the elder to overcome this situation. It automatically captures the image and beams it to the elder in their room with a beeping sound to attract the attention. The elder checks the image on the LCD monitor which is part of the Image Monitor and Authentication Module (IMAM) and takes a decision to open the door. If not satisfied with the image, the door is not opened. The elder can also have a conversation with the person outside and decide whether to permit or not. This is provided through the intercom which is attached with the PIDF. Automatically enables the GPRS to SMS and also place a call to the police and relatives. The entire IWHSS works on the assumption that the elder's health is not in bad condition. Also the elder's eyes and ears are in good condition a) Image Capture Module (ICM): This module consists of a camera and an interface to the Wi-Fi Direct wireless module. Wi-Fi Direct is a relatively new technology that allows Wi-Fi devices to talk to each other without the need for wireless access points (hot spots). The camera is placed next to the door. It is automatically activated once an object comes into the vicinity of the lens. It captures the image of the person at the entrance. The digital image is provided to the WITM and provides it to the elderly person inside the house who could view the image via an LCD Monitor attached to IMAM with a beep sound. b) Wireless Image Transmission Module (WITM): This module uses the Wi-Fi technology to transmit the captured digital images to the IMAM. The IMAM and the Security Alert Module (SAM) are inside the elder's room. The WITM and IMAM are connected by WLAN. c) Image Monitor and Authentication Module (IMAM): IMAM receives the transmitted image from the WITM and displays it to the elder via an LCD screen. The IMAM consists of a PC with Wi-Fi enabled. The elder observes the image on the monitor and decides to allow or decline the entrance of the person outside the door. d) Security Alert Module (SAM): The SAM consists of a GPRS modem attached to the PC of IMAM. It also consists of the alarm module to alert the security breach to the neighbors which is to be explained in the next section. If the elder does not identify the outsider at the entrance, he can deny permission. But if the person at the entrance does not leave the place even after a certain time also, the elder has got an option to SMS and also place a call to the police and relatives through the GPRS modem by just pressing an emergency button. This setup informs the police about the security concern at that particular house.

n at that particular house.

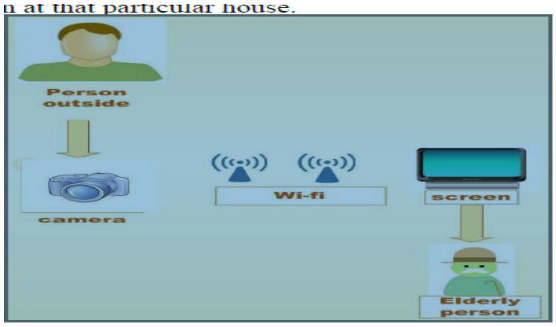
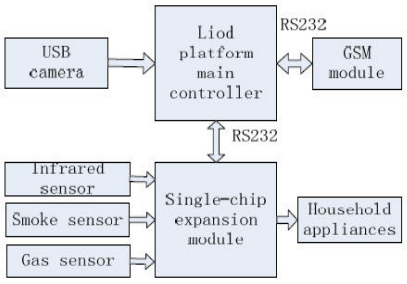


Fig.2 illustrates system 1 to know who is at the entrance

This can be employed in houses where elders live alone. Elders may not be able to stand up, walk and see through the keyhole and identify who has come at the entrance. This system helps the elderly person to identify who has come at the entrance and also to grand permission for that particular person. The main door of the house is usually attached with a calling bell.

2. DESIGN OF SMART HOME REMOTE MONITORING SYSTEM BASED ON EMBEDDED SYSTEM.

2(1) This system contains Liod platform main controller, MCS-51 Microcontrollers expansion module, GSM module, USB camera, sensor etc interface equipments

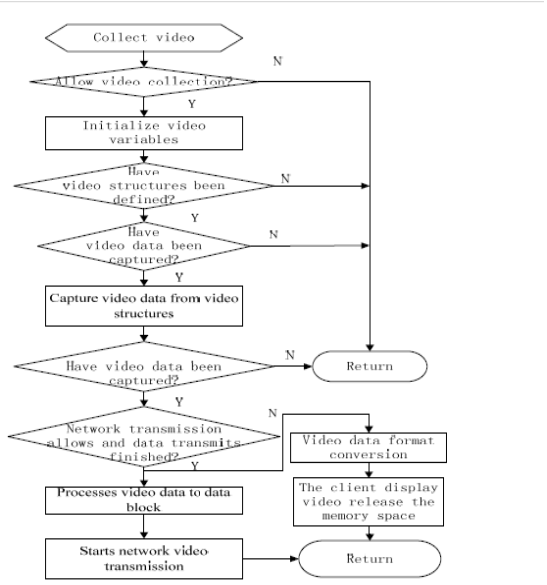


Among them, the Liod platform is system core, which mainly completes video data acquisition, analyses and processes the short messages that were received by GSM module, and controls single chip expansion module; Expansion module is mainly responsible for collecting sensor data, controlling household appliances switch, receiving and processing the control information from Liod platform, and sending feedback of sensor alarm information,household appliances switch state information to Liod platform; GSM module is used to receive short message; USB webcam is responsible for video data collection. All the surveillance information gathered by this system can be transmitted to the monitoring center server via a wireless network or cable network. Thus the system achieves effective monitoring of these statuses which endanger the safety of life and property of the people such as fire, gas leakage and illegal invasion of stranger.

Video acquisition and processing program

2(2) Video collection program was designed based on the

Open CV basic function, Open CV encapsulates the V4L related operation.[7] First the program calls cv Capture From CAM (index) function that belongs to Open CV to initialize. The index parameters are index number for USB webcam, when only one USB cameras in the system, the index is 0. Cv Set Capture Property function sets the camera resolution. Video data collection uses Open CV video to capture related operations. Firstly captures USB webcam video data into the video structures through cv Grab Frame function, secondly extracts a frame video data from video structures via cv Retrieve Frame function then processes video data to data block in network connectivity at the same time starts network video transmission Video collection program was designed based on the Open CV basic function, Open CV encapsulates the V4L related operation.[7] First the program calls cv Capture From CAM (index) function that belongs to Open CV to initialize. The index parameters are index number for USB webcam, when only one USB cameras in the system, the index is 0. Cv Set Capture Property function sets the camera resolution. Video data collection uses Open CV video to capture related operations. Firstly captures USB webcam video data into the video structures through cv Grab Frame function, secondly extracts a frame video data from video structures via cv Retrieve Frame function then processes video data to data block in network connectivity at the same time starts network video transmission



3.Research of Home Network Based on Internet and SMS Home Network architecture, which is centered on a personal computer (called HNG) connected to a GSM network/Internet and home network. This computer connects to home devices and runs a home automation management application that supervises home devices. In this paper we organize home devices into appliance, security, and messaging subsystems, respectively. The appliance subsystem consists of home appliances such as refrigerator, television

II. SUMMARY OF THE SYSTEM

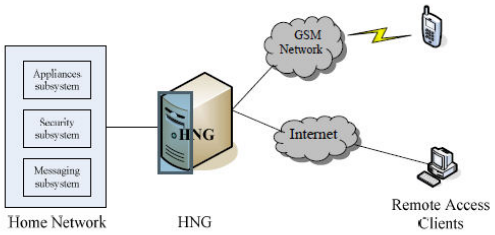
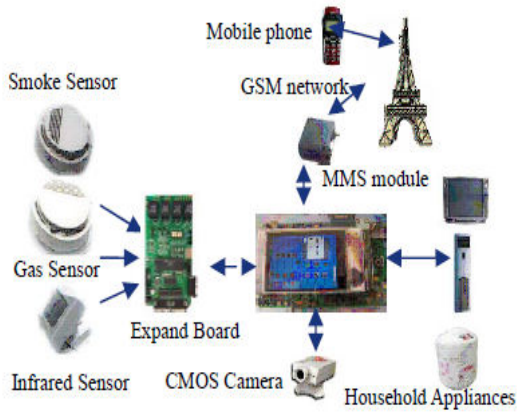


Figure 1. Home Network architeceture

4. Research of Intelligent Home Security Surveillance System Based on Zig Bee

System Architecture

Modular Design is throughout the system. Systemic built on the embedded system, and it can monitor the important position through the CMOS camera. Home state SMS and images MMS are sent to specialized mobile phones. Besides, household appliances can be remotely controlled by SMS. Zig Bee module connects household appliances, the system motherboard with smoke, temperature, gas sensors, forming a wireless networking. The system motherboard core controller is S3C44B0X-32 microcontroller and mainly responsible for dealing with the data. Through MMS modules and Zig Bee module it can send information and instructions. And Expand access plate to smoke, infrared, gas and other domestic security state sensor.



System Testing and Experimental Data Analysis

The system uses the moving target detection algorithm to achieve the targets of the surveillance image processing and abnormal judgment. Accounting for 7.5 ‰ background of the small target the system can identify. The effective elimination of the system for environmental changes in light, change the background small goals gradual movement caused by factors, such as system misjudgment. Figure 3 is the use of the system hardware and software for the intrusion detection and testing experimental picture effect

Fig3. Intrusion Detection to Results

The results show that, without obstruction in the transmission distance less than 60 m, the transmission of data packet loss rate is zero. The Test Data with No Obstruction is shown in Table 1. It can fully meet the normal home environment for the communication needs, with a low power; therefore it is very suitable for family use. If there are two cement walls between two Zig Bee modules in 30 m distance, packet loss rate is only 1 percent. And if there is one cement wall, the rate is zero, which can completely meet the requirement of system design.

5.Investigation of Security and Defense System for Home Based on Internet of Things

SYSTEM OVERALL DESIGNING

The core unit of the home security and defense system is the master controller which was selected an embedded microprocessor in the design. The microprocessor receives the alarming messages with RF communication, then sends them on to the internet with TCP/IP , so that the remote monitoring terminals are able to monitor the home security situation in time. Against the alarming of fire, gas disclosure, illegal burglary and so on, the security and defense system distributes the electronic tags with EPC along with the trouble easily happened sites that are referred to as monitoring defense region. The remote monitoring terminals can be set at community security rooms, fire departments, police bureaus or host person offices where the security and defense

situation could be monitored in time, and the emergencies would be processed as soon as possible. The block schematic of the system overall designing is shown

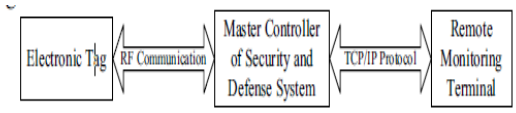
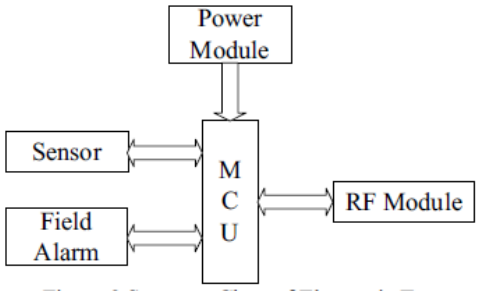


Figure 1. Block Schematic of the System Overall Designing.

The electronic tags in defense region are mainly consisted of sensors, field alarming devices, power modules, MCU and RM modules. The power module provides SCM working voltages and acts as backup power. SCM works as MCU of defense region, collects monitoring messages from sensors in real time, and when emergences happened, starts the RF modules working and gives an order to start field alarms.

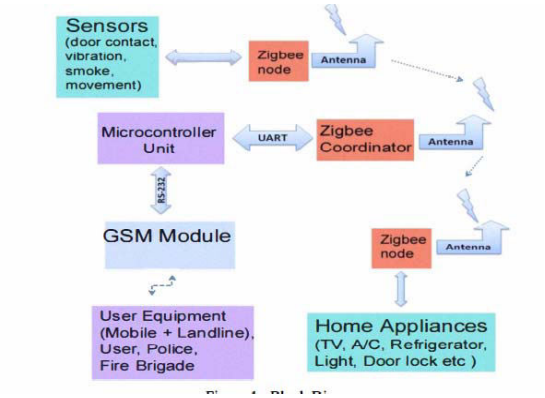


Hardware

Hardware of the system is comprised of Zig Bee EM357

module, Atmega128 MCV, Sony Ericsson T290i mobile

phone and corresponding interfaces. Zig Bee, a communication protocol, is designed to utilize the features supported by IEEE 802.15.4 radio communication standard and is implemented on the top of it. It operates in two separate frequency ranges: 868/915 MHz and 2.4 GHz and uses digital radios to allow devices to communicate. In particular the scope of Zig Bee is applications with low requirements for data transmission rates and devices with constrained energy sources. The Zig Bee network is a PAN (personal area network) network, comprises of one ZC (Zig Bee coordinator) and one or more ZEDs (Zig Bee end device) and optionally one or more ZRs (Zig Bee routers). Fabio L. Zucatto et al. in [7] compares Zig Bee with Bluetooth and narrates the significance of Zig Bee in building control wireless sensor networks. Zig Bee is a very reliable communication protocol using mesh networking topology for the reliable transmission of data between sender and receiver. The EM357 module can be installed with any sensor and home appliances as it is very small in size i.e. 21mm x 37mm,



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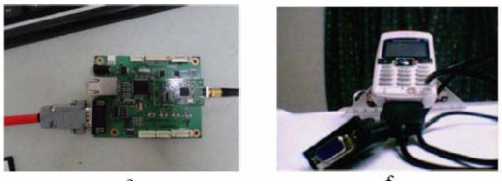


design sensors that are installed, to detect security breach, are magnetic contact sensor for sensing door opening, vibration sensor for detecting window breaking, and PIR (Passive infra-red) sensor for detecting human presence. Each sensor

and actuator is connected with ZigBee sensor node as shown in Fig 2b, 2c and 2d where EM357 ZED is connected with door contact sensor, PIR sensor, and door lock system respectively. ZigBee node continuously checks input from corresponding sensor and sends a wireless message to the Zc.

Figure 3: Serial Communication and Level Conversion between T290i and MCU

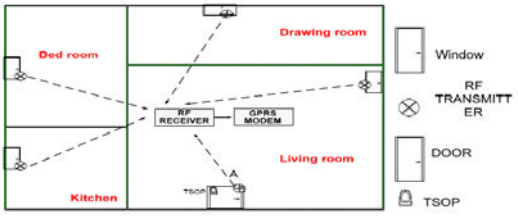
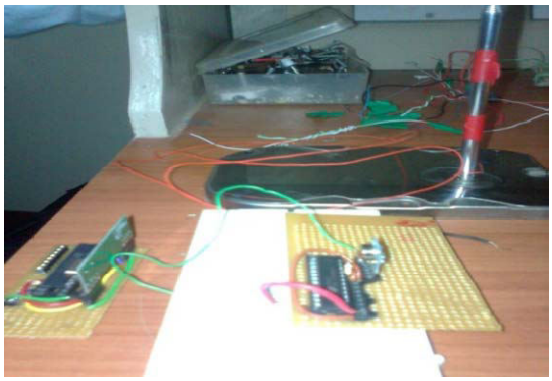


Figure 3. SBF to detect and inform theft attempt in a sample Home structure



CONCLUSION

This system adopted embedded system and singlechip extension module realizing real-time monitoring of house. This article describes the embedded smart home remote control system in the general, including the system overall design, system hardware platform and the realization of each part of interface circuit, data acquisition and processing,video acquisition and processing and GSM communication software

program realization. Overall, achieves a new smart home remote control system with real-time, practicability, compatibility.

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SECTION –II
(ADVANCED RESEARCH IN MECHANICAL ENGINEERING)

MATERIAL HANDLING EQUIPMENT OPTIMIZATION AT VOLVO GLOBAL TRUCK OPERATIONS

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Abstract— Material-handling equipment is all equipment that relates to the movement, storage, control and protection of materials, goods and products throughout the process of manufacturing, distribution, consumption and disposal. The material handling equipment used at Volvo Global Truck Operations (Volvo GTO) are reach trucks, forklifts and tow trucks. This study involve the observation of the current utilisation of the material handling equipments at Volvo GTO including the number of movement from the warehouse to the station, number of pallets, PDS trolley and kit trolley carries by the reach truck or tow truck per movement and the current routing. And identifying the areas where time and resources are wasted. And proposing a solution or an alternative to the current trend.

Keywords— *Reach trucks, Forklifts, Tow trucks, Material handling equipments, PDS (Pre Delivery System) Lead time, Routing*

I. INTRODUCTION

Material handling is the movement, protection, storage and control of materials and products throughout the process of their manufacture and distribution, consumption and disposal. This process involves a broad array of equipment and systems that aid in forecasting, resource allocation, production planning, flow and process management, inventory management, customer delivery, after-sales support and service, and a host of other activities and processes basic to business. Solutions include sophisticated techniques that expedite information flow, including RFID and satellite tracking systems, and the electronic transmission of order and shipping information. These innovations along with traditional material handling and logistics equipment and systems are the solutions that make manufacturing, warehousing, distribution and the supply chain work.

Material handling equipment is all equipment that relates to the movement, storage, control and protection of materials, goods and products throughout the process of manufacturing, distribution, consumption and disposal. Material handling equipment is the mechanical equipment involved in the complete system. Material handling equipment is generally separated into four main categories: storage and handling equipment, engineered systems, industrial trucks, and bulk material handling.

Storage and handling equipment is a category within the material handling industry. The equipment that falls under this description is usually non-automated storage equipment. Products such as pallet racking, shelving, carts, etc. belong to storage and handling.

Engineered systems are typically custom engineered material handling systems. Conveyors, Handling Robots, AS/RS, AGV and most other automated material handling systems fall into this category.

Industrial trucks usually refer to operator driven motorized warehouse vehicles, powered manually, by gasoline, propane or electrically. Industrial trucks assist the material handling system with versatility; they can go where engineered systems cannot.

Bulk material handling equipment is used to move and store bulk materials such as ore, liquids, and cereals. This equipment is often seen on farms, mines, shipyards and refineries.

Volvo GTO being a manual assembly plants uses pallets and bins for storage of the raw materials. And industrial trucks such as forklifts, reach trucks and tow trucks for the transportation of the materials from the storage area to the assembly line.

The forklifts are used to lift heavy parts such as engine- gearbox assembly, front and rear axle from the loading bay to the respective station. While reach trucks are used to carry pallets from the warehouse to the stations. And tow trucks are used to tow kit trolleys and PDS trolleys from the warehouse to the assembly line.

The Bill of Material at Volvo GTO is issues batch-wise of 10 trucks for FMX models and 20 trucks for FM and FH models. The warehouse issues the materials at the rate of 10 trucks per day. And supply of material the consecutive day depends on the rate of production that may vary from 4-8 trucks per day.

II. OBJECTIVE

Perform analysis of material handling equipments and methods in Chassis, Power Train and Cab Trim assembly lines. And to categorise all types of equipments used. Also to identify the assembly line in which material handling equipments and vehicles are not efficiently used. And recognise different ways to reduce the distance travelled by the reach truck and tow truck. And finally to determine the possible

distribution of the material handling equipments such that minimal movement is done for the transportation of the material from the warehouse to the respective line.

Shop floor data over the past one month was analysed and the material delivery to Chassis, Power Train and Cab Trim assembly lines was observed. They were then sorted according to the equipments used and were categorised into the following categories:

Equipments
- •Reach Truck
- •Tow Truck
- •Forklift

Containers
- •Pallet
- •Bins
- •Kit
- •PDS (Pre Delivery System) Trolley

III.DATA COLLECTED

The collected and categorized data was then entered into a table that showed the distribution of parts in bins, pallets and kit. And the number of movement of the tow truck, reach truck and forklift was determined and recorded in Table 1 and the departments and their corresponding station numbers are shown in Table 2.And number and the percentage of parts transported to different department by different modes are shown in Table 3 and Fig.1 respectively.

TABLE I PARTS DISTRIBUTION AT DIFFERENT LINES

CRITERIA	BIN	PALLET	KIT
Cab Trim	10	59	14
Cab Trim Pre Assembly	5	0	16
Chassis Line	25	72	1
Power-train Pre Assembly	1	35	60

TABLE 2 ASSEMBLY LINES AND CORRESPONDING STATION NUMBER

Line	Station No:
Cab Trim	8101,8102,8103,8014&69000
Cab Trim Pre Assembly	2710,8810&60100(Partial)
Chassis Line	60000,60050,60100,60150,60200,60250,60300,60350&60400
Power-train Pre Assembly	65000(Engine), 67200(Rear axle), 67000,67100(Front Axle), 68000(Valve), 68800(PI Pipe) and 66600(Radiators and exhaust).

TABLE 3 -NUMBER OF PARTS DISTRIBUTED IN EACH MODE OF TRANSFER

Type of transfer	No: Of Parts	Remarks
PDS (Pre Delivery System) Trolley	927	PDS (Pre Delivery System) trolley is used to transfer fasteners and washers
Bins	41	Used to hold small parts such as brackets, etc.
Pallet (Reach Truck)	166	Large parts
Kit	91	Used for small parts incase of batch in production
Forklift	3	Used to transport very heavy parts such as engine and axle.

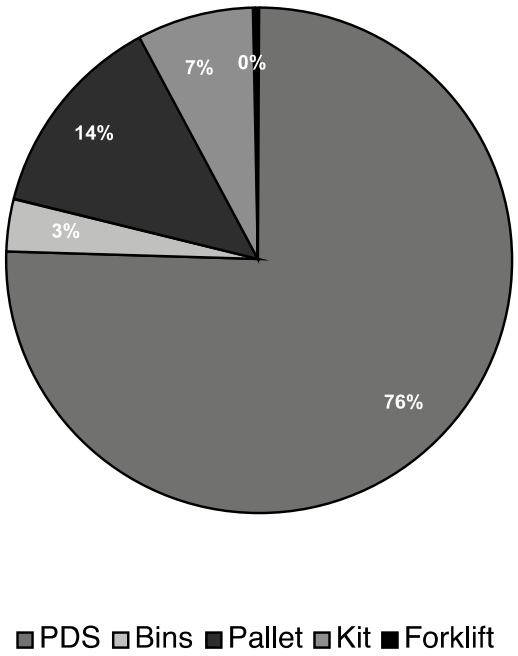


Fig. 1 Percentage of parts transported by different equipments

And the number of pallets, PDS trolley, and kit trolley required for each station was observed and tabulated in Table 4.

TABLE 4- NUMBER OF PALLETS, KIT AND BINS AT EACH ASSEMBLY LINE

Department	No: of Pallet (Reach Truck)		No: of Kit		No: of Bins
	No: of collars	No: of Pallet	PDS (Pre Delivery System)	Kit	
Cab Trim	1	25	1	7	-
	2	9			
	3	13			
	4	2			
	Crate	2			
Cab Trim Pre Assembly	1	-	1	2	3
	2	-			
	3	2			
	4	-			
	Crate	-			
Chassis Line	1	36	8	8	19
	2	10			
	3	3			
	4	3			
	Crate	4			
Power-train Pre Assembly	1	14	3	4	3
	2	18			
	3	10			
	4	5			
	Crate	6			

Also the number of movements done by different equipments per batch of 10 trucks has been tabulated in Table 5.And time take for the material handling equipments to travel from the warehouse to the different department and back has been shown in Table 6

TABLE 5- NUMBER OF MOMENT PER BATCH OF 10 TRUCKS

Department	Number of moment per batch of 10 trucks		
	Reach Truck	Forklift	Tow Truck
Cab Trim	41	-	9
Cab trim pre assembly	3	-	3
Chassis Line	22	10	18
Power-train pre assembly	55	6	20

TABLE 6- TIME TAKEN FOR A SINGLE MOMENT FROM AND TO WAREHOUSE (MIN)

Department	Time taken for a single moment from and to warehouse (min)		
	Reach Truck	Forklift	Tow Truck
Cab Trim	6	-	5
Cab trim pre assembly	6	-	5
Chassis Line	6	7	6
Power-train pre assembly	5	7	4

The routes taken by the vehicle to different stations from the warehouse is shown in Fig.2.

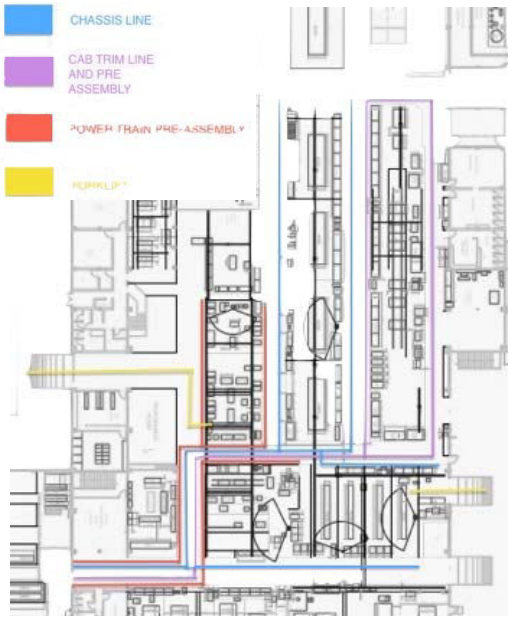


Fig. 2 Current routes from the warehouse to different stations.

And the distance between the warehouse and the departments is shown in Table 7.

TABLE 7- DISTANCE FROM WAREHOUSE IN METERS

Station no:	Distance from warehouse in meters

Station no:		Distance from warehouse in meters
8101	Cab trim department	130
69000		160
60000		88
60250	Chassis assembly	98
60400		158
65000	Power train pre-assembly	86
66200		110
67200		75

IV. PROBLEMS IN THE CURRENT USAGE OF THE MATERIAL HANDLING EQUIPMENTS

After the data collection, the following observations were made.

•The reach and the tow truck to reach the cab trim pre-assembly travel an extra distance of 115meters.

•2 minutes is taken by the truck to travel the extra distance.

•The trucks due to the volume limitations in the reach truck transport only 7 single collar pallets.

•The movement of trucks between the stations and the warehouse is increased because of the less volume of materials transported per trip.

•The material handling equipments are not efficiently used.

•Gangway width of 3.2 meters is not suitable for the tow truck to tow multiple kits at once.

V. PROPOSED MATERIAL HANDLING TRENDS AND ROUTES

Material handling equipments can be used in an optimum way by

•Reducing the distance travelled.

•Reducing the number of movement.

•Empty trucks during return to the warehouse.

The above requirements can be met by using the following change in the current trend and the route:

1.The length of the forks of the forklift when increased by 400 mm and the orientation of the pallets carried is changed from lengthwise to breadthwise as shown in picture below, will lead to the increase in the carrying capacity of the truck by twice the amount, which implies that the number of movement is halved. But design specifications of the forklift has to be changed as there will be a shift in the center of gravity of the forklift which can topple the truck and this can be rectified by altering the position of the counter weight. And the design of the pallet racks has to be modified in order to hold the pallet at the stations, as shown in Fig.3

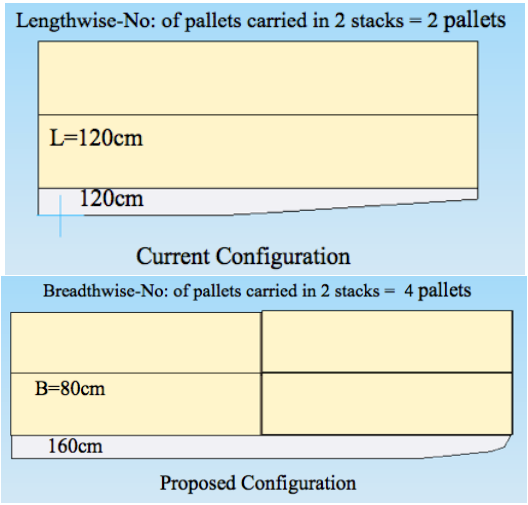


Fig. 3 Proposed orientation of the pallets in the reach truck and new proposed design of the forks of the reach truck.

2.When the carrying capacity of the reach truck is increased the unnecessary path in the normal route from station 69000LHS to 69000RHS(total distance for 2 complete movement=490m) can be avoided, when the proposed route (distance for 2 complete movement=375m) thus reducing the distance travelled by 115 m. As shown in Fig.4

Fig. 4-The proposed change in route from station 69000LHS to 69000RHS

3. Having an increase in the gangway only at the corners will increase the turning radius of the tow truck thus increasing the number of kits towed, reducing the number of movements of the tow truck and reduction in the distance travelled.Fig.5 shows the current and the proposed geometry of the gangway.And Table 8 shows the difference in the number of movements of the tow truck.

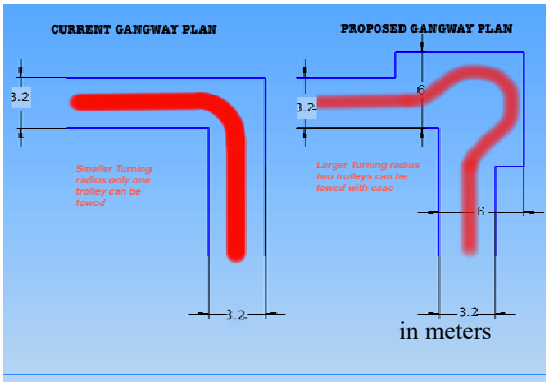
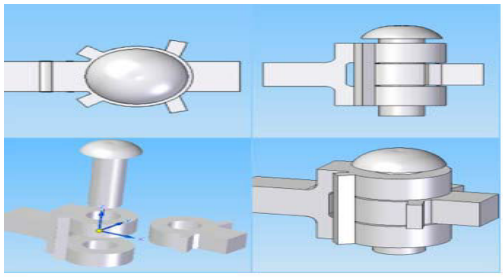


Fig. 5 Proposed and current geometry of the Gangway.

TABLE 8- TIME TAKEN FOR A SINGLE MOMENT FROM AND TO WAREHOUSE (MIN)

Department	Number of moment of tow truck per batch of 10 trucks	
	Current Gangway Plan	Proposed Gangway Plan
Cab Trim	9	5
Cab trim pre assembly	3	2
Chassis Line	18	9
Power-train pre assembly	20	10

4.The turning radius of the tow truck can be reduced in comparison by changing the type of coupling on the trolley from the current coupling used. And a barrier or restriction is used to avoid oversteering of the kits and avoid the kits crashing into the tow truck.



Proposed Coupling

Current Coupling

Fig. 6 Proposed and current geometry of the Gangway.

VI. CONCLUSIONS

The optimization of material handling equipments has been successfully carried out on the three chosen assembly lines. The current distribution and utilization of the material handling equipment such as reach truck, forklift and tow truck was identified and assessment was made on the observations.

An alternate route was found to reduce the traveling distance of the vehicles. And certain changes were proposed to increase the efficiency of the said equipments. The changes in the gangway and the coupling will increase the amount of trolleys towed by the tow truck, and the changes to the fork of the reach truck will reduce the traveling distance by 115meters, and the changes made to the coupling will double the material carrying capacity of the tow truck to 2 trolleys.

ACKNOWLEDGEMENT

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A PERFORMANCE EVALUATION OF LEAF SPRING REPLACING WITH COMPOSITE LEAF SPRING

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Abstract - The automobile industry has shown increased interest in the replacement of steel spring with fibre glass composite leaf spring due to high strength to weight ratio. Therefore the aim of this work is to reduce the weight and low cost fabrication of complete mono composite leaf spring and mono composite leaf spring with bonded end joints. Also, general study on the analysis and design. A single leaf with variable thickness and width for constant cross sectional area of unidirectional glass fibre reinforced plastic (GFRP) with similar mechanical and geometrical properties to the multi leaf spring, was designed, fabricated (hand- layup technique) and tested. The results showed that an spring width decreases hyperbolically and thickness increases linearly from the spring eyes towards the axle seat. The finite element results using ANSYS software showing stresses and deflections were verified with analytical and experimental results. The design constraints were stresses (Tsai-Wu failure criterion) and displacement. Compared to the steel spring, the composite spring has stresses that are much lower, the natural frequency is higher and the spring weight is nearly 85 % lower with bonded end joint and with complete eye unit.

Keywords:- *composite, glass fibre reinforced plastic (GFRP),*

I. INTRODUCTION

In order to conserve natural resources and economize energy, weight reduction has been the main focus of automobile manufacturer in the present scenario. Weight reduction can be achieved primarily by the introduction of better material, design optimization and better manufacturing processes. The suspension leaf spring is one of the potential items for weight reduction in automobile as it accounts for ten to twenty percent of the unsprung weight. This helps in achieving the vehicle with improved riding qualities. It is well known that springs, are designed to absorb and store energy and then release it. Hence, the strain energy of the material becomes a major factor in designing the springs.

The relationship of the specific strain energy [3] can be expressed as

$$U=\sigma^2/\rho E$$

Where, σ is the strength

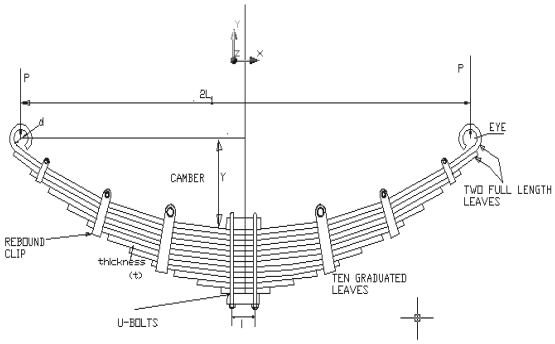
ρ is the density

E is the Young's modulus of the spring material.

It can be easily observed that material having lower modulus and density will have a greater specific strain energy capacity. The introduction of composite materials was made it possible to reduce the weight of the leaf spring without any reduction on load carrying capacity and stiffness [1].

In every automobile, i.e. four wheelers, trucks the leaf spring is one of the main components and it provides a good suspension and it plays a vital role in automobile application. It carries lateral loads, brake torque, driving torque in addition to shock absorbing. The advantage of leaf spring over helical spring is that the ends of the spring may be guided along a definite path as it deflects to act as a structural member in addition to energy absorbing device [2].

II. GEOMENTRY OF SPRING



III. LITERATURE SURVEY

- Rajendran studied the application of composite structures for automobiles and design optimization of a composite leaf spring. Great effort has been made by the automotive industries in the application of leaf springs made from composite materials.
- S. Vijayarangan showed the introduction of fibre reinforced plastics (FRP) made it possible to reduce the weight of a machine element without any reduction of the load carrying capacity. Because of FRP materials high elastic strain energy storage capacity and high strength-to-weight ratio compared with those of steel, multi-leaf steel springs are

being replaced by mono leaf FRP springs .

- H.A. Al-Qureshi study on the analysis, design and fabrication of composite springs. From this viewpoint, the suspension spring of a compact car, "a jeep" was selected as a prototype. A single leaf, variable thickness spring of glass fiber reinforced plastic (GFRP) with similar mechanical and geometrical properties to the multi leaf steel spring, was designed, fabricated (moulded and hoop wound) and tested. The testing was performed experimentally in the laboratory and was followed by the road test. Comparison between the performance of the GFRP and the multi leaf steel springs is presented. In addition, other relevant parameters will be discussed [8].

- Mouleeswaran Kumar This paper describes static and fatigue analysis of steel leaf spring and composite multi leaf spring made up of glass fibre reinforced polymer using life data analysis. The dimensions of an existing conventional steel leaf spring of a light commercial vehicle are taken and are verified by design calculations. Same dimensions of conventional leaf spring are used to fabricate a composite multi leaf spring using E-glass/Epoxy unidirectional laminates. The load carrying capacity, stiffness and weight of composite leaf spring are compared with that of steel leaf spring analytically and experimentally.

A. DEFINITION

Composite A composite is a structural material that consists of two or more combined constituents that are combined at a macroscopic level and are not soluble in each other. One constituent is called the *reinforcing phase* and the one in which it is embedded is called the *matrix* [3]. The reinforcing phase material may be in the form of fibers, particles, or flakes. The matrix phase materials are generally continuous. Examples of composite systems include concrete reinforced with steel and epoxy reinforced with graphite fibers, etc [2].

B. CLASSIFICATION

Matrix Based [5]

- Polymer Matrix Composites
- Metal Matrix Composites
- Ceramic Matrix Composites

Reinforcement Based

- Fiber Reinforced Composites
- Whisker Reinforced Composites
- Particle Reinforced Composites

III. LEAF SPRING

The spring is a machine part used to absorb sudden loads and to accumulate elastic energy [3]. There are different mechanical designs and forms of springs [2]. The spring under consideration is called a *leaf spring.* A typical leaf spring is shown in Figure shows the leaves hold together by a (1) centre bolt and (2) clamp. Fig. show different spring ends used in practice. The top leaf is designated as the main leaf. fig. shows various parts of the of leaf spring

Leaf spring:
(a) Spring (1, centre bolt; 2, clamp),
(b) Eye spring end, and
(c) Plain spring end.

IV. DESIGN PARAMETER OF STEEL LEAF SPRING

Parameters of the steel leaf spring used in this work are shown in Table 1
The expression for bending stresses [6],

$$S = \frac{l\,t}{2\sum I} P$$

The deflection, given by

$$f = \frac{Pl}{2E\ SF\ \sum I}$$

Appro. Mass of spring is given by

M = (one half of spring length *SF) (Unit mass from table)/1000

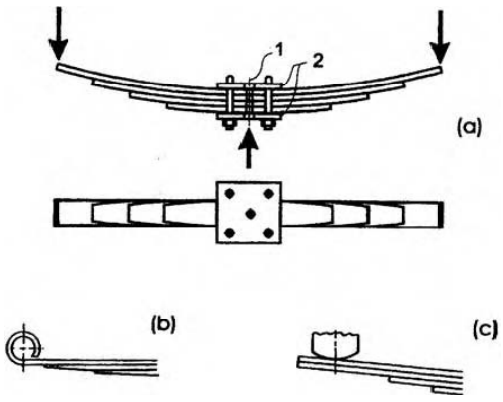


TABLE 1

Parameter	Value
Material selected-Steel	55Si2Mn90
Tensile strength (N/mm^2)	1962
Yield strength (N/mm^2)	1470
Young's modulus E (N/mm^2)	2.1*10^5
Design stress (σ_b) (N/mm^2)	653
Total length (mm)	1190
The arc length between the axle seat & the front eye(mm)	595
Arc height at axle seat (mm)	120
Spring rate (N/mm)	32
Nominal static loading (N)	3850
Available space for spring width (mm)	60-70
Spring weight (kg)	26

V. ANALYSIS OF COMPOSITE LEAF SPRING

To design composite leaf spring, a stress analysis was performed using the finite element method done using ANSYS software. Analysis carried out for composite leaf spring for Glass/Epoxy, Graphite/Epoxy and Carbon/Epoxy composite materials and the results were compared with steel leaf spring.

For steel leaf spring

Boundary condition: - In this analysis is one end is assumed to be fixed and loading is
applied at other end. A finite element stress analysis is performed under full bump loading [9].

- Element type & density:- every leaf with eight-node 3D brick element (solid 45)
- five-node 3D contact element (contact 49)

For composite leaf spring

Element type & density for mono composite leaf spring [5]: - eight-node 3D SOLID46.

(For multi leaf spring to establish contact between the leaves, the interface elements CONTACT174 and TARGET170 are chosen.)

Figs. represent FEA results for steel and mono composite leaf spring (Glass/Epoxy) [5].

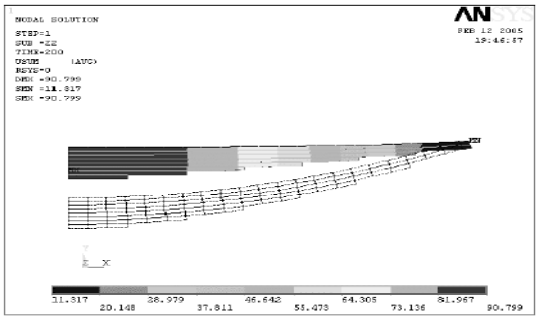


Fig.5.1 Displacement pattern for steel leaf spring

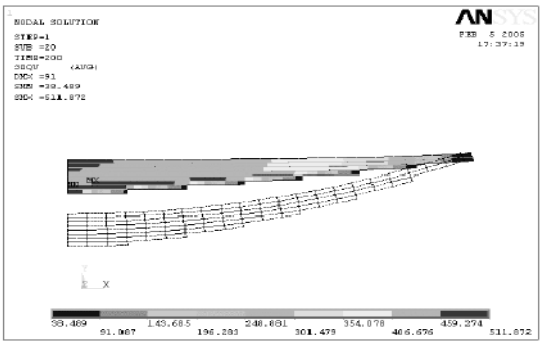


Fig.5.2 shows Stress distribution for steel leaf spring [9].

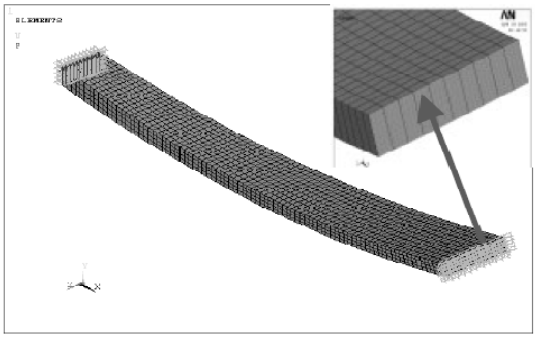
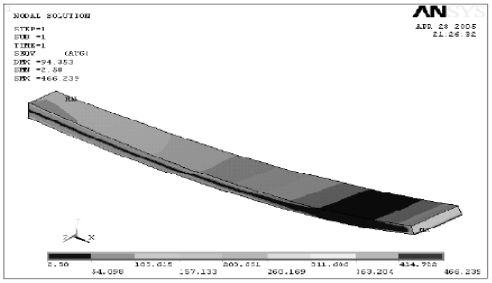


Fig.5.3 show Boundary conditions and meshed model of mono Composite leaf spring [9].



MATERIAL	STATIC LOAD (N)	MAX.DEFLECTION (mm)		MAX.STRESSES (Mpa)		WEIGHT (Kg)
		FEA	*Numerical*	*FEA*	*Numerical*	
Steel	3980	90	107.5	511	653	26.0
E-glass/ Epoxy	4250	94	105.0	466	473	3.88
Graphite/Epoxy	-	68	-	422	-	2.33
Carbon/Epoxy	-	62	-	413	-	2.39

Fig.5.4 shows Stress distribution for Glass/Epoxy composite mono leaf spring

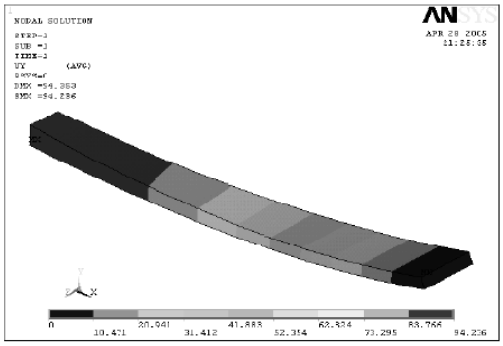


Fig5.5 show Displacement pattern for Glass/Epoxy composite leaf spring [9].

VI. ESULT DISCUSSION

Numerical results of the leaf spring under static loading containing the stresses and deflection are listed in the Table. These results are also compared with FEA in Table. Since the composite leaf spring is able to withstand the static load, it is concluded that there is no objection from strength point of view also, in the process of replacing the conventional leaf spring by composite leaf spring. Since, the composite spring is designed for same stiffness as that of steel leaf spring, both the springs are considered to be almost equal in vehicle stability. The major disadvantages of composite leaf spring are chipping resistance.

- The weight of the leaf spring is reduced considerably about 85 % by replacing steel leaf spring with composite leaf spring. Thus, the objective of the unsprung mass is achieved to a larger extent. The stresses in the composite leaf spring are much lower than that of the steel spring.
- From the results, it is observed that the composite leaf spring is lighter and more economical than the conventional steel spring with similar design specifications.

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AIRCRAFT CONTROL SURFACE OPTIMIZATION

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Abstract--This paper describes the conceptual optimization as performed on an aileron from a typical supersonic aircraft. The goals were to re-design an existing configuration maintaining the overall stiffness, weight and also reducing the manufacturing cost. A design methodology has been developed to rapidly generate the basic structural configurations to meet given performance requirements. These requirements are either transformed into constraints or an objective function during the optimization process. ANSYS and Nastran has been used throughout the optimization process starting with a topological optimization study to determine basic internal lay-outs. The internal configuration was then decided concurrently by examining structural and manufacturing constraints. This was followed by parametric optimization carried out on a stepwise fashion to determine firstly the optimum position of internal ribs and spars and finally the optimum skin thickness in each bay. Different initial configurations were studied to determine whether a spar / rib dominated design would be most suitable for the given structure. Additional internal configurations proposed on the basis of minimum assembly/manufacturing cost were quickly analyzed using ANSYS and Nastran parametric capabilities.

Keywords—*Control Surface Optimization, FEA, Ansys , Nastran Techniques.*

I. INTRODUCTION

The main goals of this START Grant Program were to develop innovative design and manufacturing technologies for composite control surface structural components that can be used on new passenger and military aircraft. Design of control surfaces requires consideration of a number of constraints based on structural performance and manufacturing considerations. Some of those structural requirements are stiffness related such as buckling performance, maximum displacements and aerodynamic smoothness. Usually strength requirements can be met by achieving the required stiffness. From a manufacturing point of view; and for unitized construction; the number of internal mandrels required to produce the control surface can usually yield a relative cost comparison between different structural lay-outs.

Standard design methodology operates on the assumption of an internal configuration at the conceptual design stage followed by analysis. Compliance to structural requirements is subsequently assessed and assumptions can be made as to possible further changes needed to achieve compliance. This iterative process can become quite lengthy and is widely known as “trial and error” methodology. Once the compliance is achieved detail analysis can be completed. The coupling of

Topological and Parametric capabilities within ANYS allow for a different methodology to be proposed. This methodology can yield results significantly faster when compared to standard practice. Efficiency ratios of 10:1 (proposed: standard methodology) were achieved in work performed under this task.

II. DESIGN OPTIMIZATION METHODOLOGY

Design Optimization methodologies were previously studied by various researchers within organizations with whom Hawker de Havilland collaborates (References 1, 2, 3). Also more recently other studies (References 4, 5 & 6) were published as a result of this and other structural optimization activities.

The Design Optimization Methodology proposed consists in performing topological optimization to determine basic structural lay-out based on critical loading cases. Topological optimization provides an indication of load paths and as a result it indicates where material is mostly needed. A desired material reduction can be achieved while maximizing global stiffness (minimizing compliance). Its drawback is that results require; in some cases; significant interpretation, thus coarse meshes are not recommended. The interpretation stage can also be aided by the concurrent engineering approach of bringing expert manufacturing knowledge to this critical decision stage. Drawing on this knowledge can provide a number of preferred manufacturing solutions that can then be married to topological results. A number of compromises can then be suggested as internal layouts. Once these suggested internal layouts are agreed to, after trade-off studies, a parametric optimization is carried out to determine the optimum position of the internal ribs and spars. This is considered to be a key advantage of the ANSYS parametric engine as it allows assessment of large design spaces due to its automatic re-meshing capabilities.

A further parametric optimization is carried out to determine optimum thickness distributions for the different bays. It was found that the stepwise approach to determining internal member positions

followed by determination of optimum thicknesses yielded faster results convergence and provided more insight into the structural behavior of the control surface studied. The importance of a better understanding of the design space and the achievement of a robust design can't be overstated. Whereby the standard methodology might result in an efficient solution for the given conditions, any change in those conditions can result in lengthy re-analysis to assess compliance. This is not the case for the proposed Design Optimization Methodology whereby changes can be quickly implemented and in some cases, given the insight into the structural behavior of the part, an analysis run might not be at all required. A typical flowchart of this methodology is shown on Figure 1.

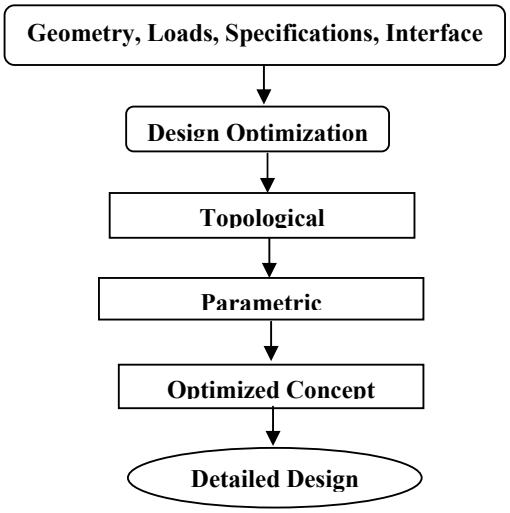

Figure 1 - Typical Design Optimization Methodology Flowchart

1. GEOMETRY, LOAD CASE AND MATERIAL PROPERTIES

The aileron studied had an average chord of 20 in., an average span of 150 in. and the front spar depth was approximately 4 in.

2. LOAD DISTRIBUTION

The single load case applied is shown in Figure 2. The load case applied is best represented by a triangular distribution with its peak at the aileron's hinge line tapering to zero at the tab hinge line. Air loads were applied evenly (50/50) on both upper and lower skins. Tab loads were resolved to five (5) tab hinge locations. Constraints and enforced displacements were applied to aileron hinge locations. Enforced displacements were imposed at all hinge positions to simulate wing bending.

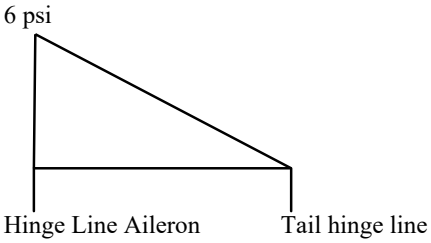

Figure 2 - Pressure distribution

3. MATERIAL PROPERTIES

Lamina and Laminate properties employed in the FEA analysis of the aileron are shown on Tables 1 & 2 respectively. Laminate properties are based on a quasi-isotropic lay-up of 12 plies.

Table 1: Lamina properties Original Material and New Material

	Original Material	G926/M18
E11 (MPa)	5.78E+04	7.00E+04
E22 (MPa)	5.78E+04	7.00E+04
G12 (MPa)	3.10E+03	3.90E+03
□12	0.03	0.04

Table 2: Laminate properties Original Material and New Material

	Original Material	G926/M18
E11 (MPa)	4.09E+04	4.96E+04
E22 (MPa)	4.09E+04	4.96E+04
G12 (MPa)	1.56E+04	1.88E+04
□12	0.313	0.32

These laminate properties were assumed to be of isotropic nature for the purposes of the optimization run.

4. ANALYSIS

Topological and Parametric Optimization was conducted using ANSYS Workbench v 12.0.1. The combined Air Load and Sympathetic bending case employed for all finite element analysis runs is referred to in the Geometry, Load Case and Material Properties section. The finite element model employed in the analysis is depicted in Figure 3. The re-design activities consisted on achieving similar stiffness characteristics to the original aileron while reducing the manufacturing cost. The original aileron is produced with honeycomb stiffened panels whereas the re-design intends to replace these panels with a unitised co-cured structure consisting of solid composite panels with ribs and spars.

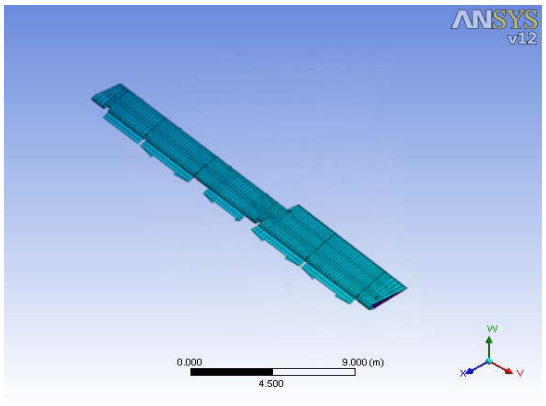

Figure 3 - Finite Element Model

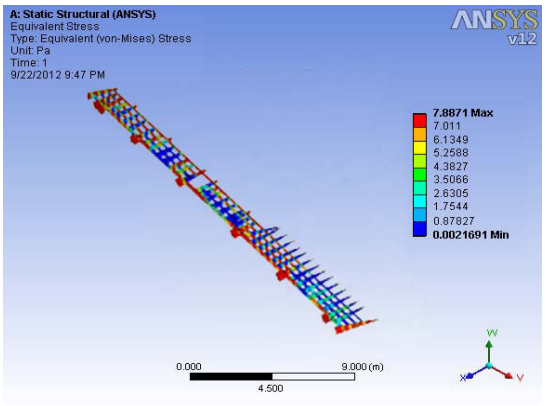

Figure 4 - Pseudo-densities Plot

III. TOPOLOGICAL OPTIMIZATION

This is usually referred to as "layout" optimization. The goal is to achieve a "maximum stiffness" design while reducing the material needed. The objective function in this case is to minimize the energy of structural compliance while satisfying a volume constraint. The design variables in this case are the pseudo-densities of each finite element. For the aileron the volume reduction was set at 50%. The value chosen for the reduction is a trade-off between time to solve and increased structural definition. That is the larger the volume reduction chosen, the more definite the load path will appear and vice-versa. The aileron was fully populated with internal ribs and spars so as to employ the results to define the members that would be most efficient in transferring the load from the hinges into the torsion box. SHELL 93 elements were employed for the topological studies. All internal members were assigned equivalent thicknesses so as to avoid any bias. Hinges and closing ribs were specified as non-optimized regions by identifying those elements as TYPE 2 elements. After completing the run, the pseudo-densities were plotted and discussed with people whose manufacturing expertise aided in assessing cost implications of choosing the different possible designs. The plot showing the pseudo-densities yielded by the topological optimization study are shown in Figure 4. Although decisions made at this stage are very significant as they can skew the design one way or another, ANSYS parametric capabilities allow for the inclusion of internal members whose efficiency is questionable. This is achieved by planning ahead all possible combinations that are to be studied and creating the areas representing these members without meshing them. Therefore the subsequent inclusion of these members in future optimization runs is achieved by simply modifying a few lines on the input files.

Once the suggested internal layout is agreed to, a parametric optimization is carried out to determine the optimum position of the internal ribs and spars. The layout chosen based on input from the structural analysis and on manufacturing experience (cost) is shown in Figure 5. The configuration depicts a front spar, one mid spar and a rear spar. The rear spar was initially considered to be continuous (full span). However it was later noted that no buckling modes were present in this area. The mid-spar is discontinuous due to cut-outs on the centre area of the aileron to allow for the tab actuator. Although two mid spars seem to be required based on topological results, it was decided to employ one thicker mid spar to minimize manufacturing costs. Ribs were extended from most hinges up to mid spar. This is mostly based on topological results and it provides the added advantage of minimizing mandrel counts for a unitized aileron.

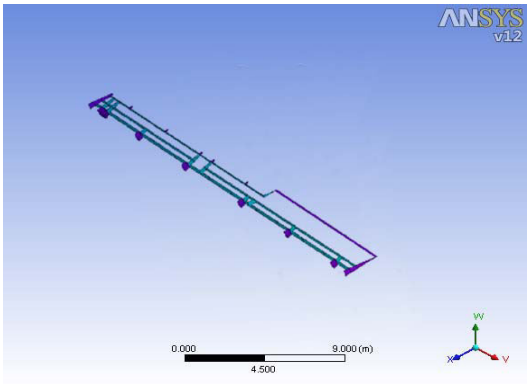

Figure 5 - Internal Lay-out

IV. PARAMETRIC OPTIMIZATION

SHELL 63 elements were employed throughout the parametric optimization studies. The design objective pursued throughout the parametric optimization was to minimize buckling (maximise1st Mode Eigenvalue). In the first instance the position of the mid-spar was chosen as the single design variable. It is important to note that the overall aileron

geometry and load pick-up locations (Outer Mould Line (OML), hinge and tab hinge locations, structure forward of front spar) could not be modified as the aileron needed to interface with existing structure and also due to aeroelastic issues. A plot of the 1st Eigenvalue previous to the first parametric optimization run and a fringe plot depicting out of plane displacement are shown on Figures 6 & 7. Convergence was achieved very rapidly after only 6 iterations resulting in an increase in 1st Mode Eigenvalue of approximately 25%. This increase in Eigenvalue was achieved by modifying the mid spar position by only 0.6 inches. A plot showing the optimization history is shown in Figure 8. The weight changes during this optimization run are negligible since the skin thickness for all bays are equal, thus the weight change is given by the change in mid spar height only.

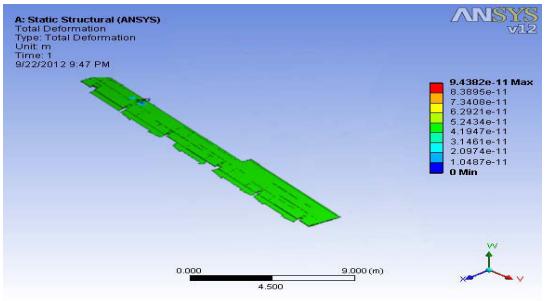

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Figure 6 - 1 Eigenvalue Pre-Optimisation Run

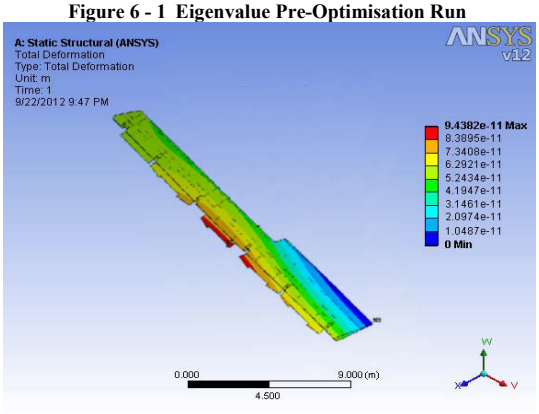


Figure 7 - Displacement Fringe Plot

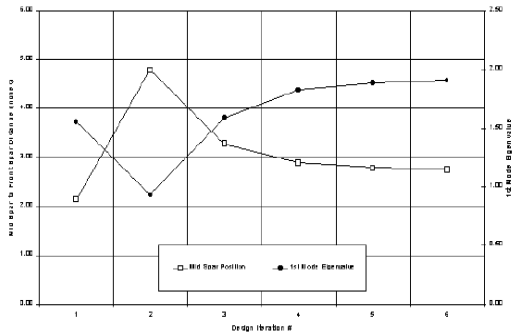


Figure 8 - Spar Optimization Iteration History

This study was followed by thickness optimization whereby an upper and lower constraint was placed on the 1st Mode Eigenvalue (0.8 to 1.0) while the design objective was set as a minimum weight design. In this case the weight was reduced by up to 20 %. A relative wide range had to be placed between upper and lower limits on the 1st Mode Eigenvalue in order to avoid overly constraining the optimization run. The optimization run converged after 8 iterations. The optimization history for this study is shown on Figure 9. An appropriate thickness based on manufacturing constraints (composite ply thickness) was then chosen. The optimum number of plies yielded by the analysis was 4.75 plies of the "New Material" (0.352 mm/ply) and this was rounded up to 5 plies. A plot of the 1st Eigenvalue and a fringe plot depicting out of plane displacement at the completion of the parametric optimization studies and after rounding up to allow for manufacturability are shown on Figures 10 & 11.

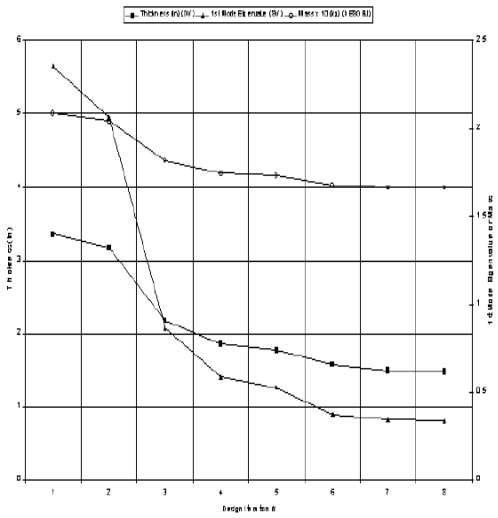
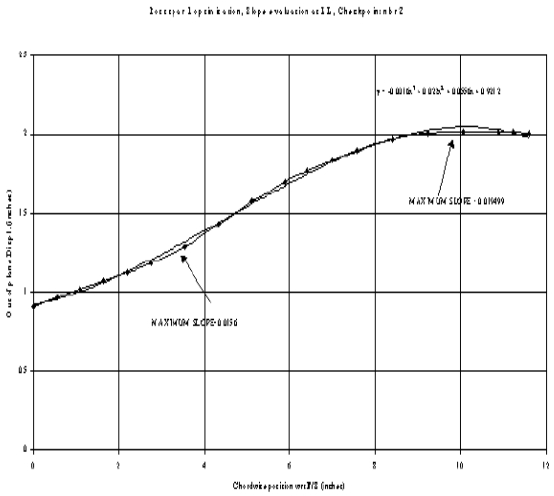


Figure 9 - Thickness Optimization Iteration History



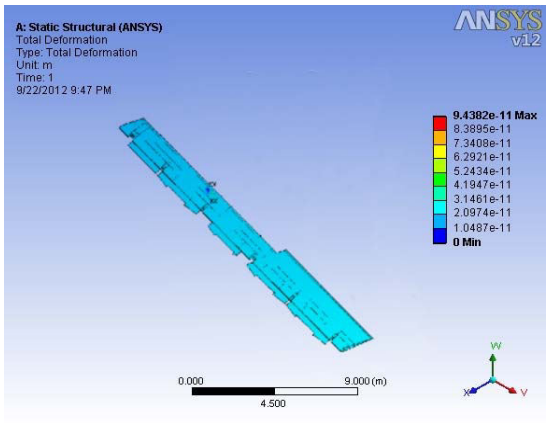


Figure 10 - 1st Eigenvalue Post-Optimization Run

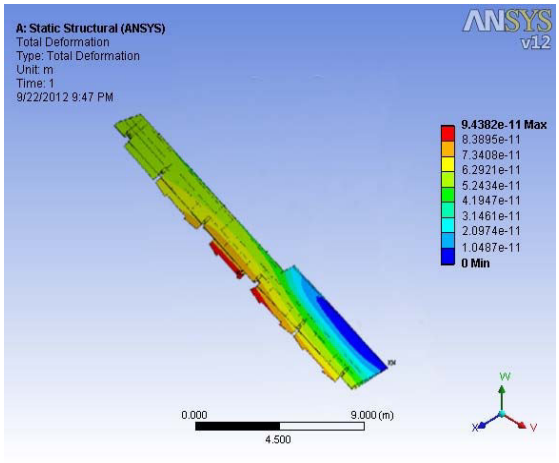


Figure 11 - Displacement Fringe Plot Post Optimization

V. ANALYSIS RESULTS & DISCUSSION

Aerodynamic smoothness was also checked at the end of the optimization run to ensure all technical requirements were met. This was achieved by fitting a cubic polynomial equation to the out of plane displacements along a critical span wise location. The cubic polynomial equation represents the mean outer skin profile. The maximum mean slope can be calculated by dividing the wave amplitude by the half wavelength of the actual skin profile. A plot of the actual and mean skin profiles for slope calculation is shown on Figure 12.

Based on the depicted internal structure, two designs were further assessed employing the two chosen materials as per Tables 1 & 2 (Original Material and New Material). The thickness for skins and internal structure of the "New Material" and "Original Material" designs is shown on Table 3.

A result matrix comparing these two designs against technical requirements is shown on Table 4. Weight calculations assume a monolithic construction, thus includes a weight saving of an estimated 1.2 kg for fasteners employed in the aft box.

The complete process of analyzing and optimizing the aileron took only 12 days. A large number of options were studied within this period. This is considered to be a significant improvement when compared to the standard methodology of "trial and error" previously employed. The insight gained throughout the analysis also provides opportunities for future analysis of control surfaces either where redesign is concerned or for new projects.

Table 3: New Material and Original Material Ply stack-up for skins and internal structure

PARAMETRIC OPTIMISATION PARAMETERS		
New Material	Original Material	
Thickness	Thickness	Description
(inches)	(inches)	
0.1247	0.1299	Top & bottom skin leading edge
0.3326	0.3291	Top & bottom skin front spar flange region
0.0416	0.0433	Top skin F/S to Spar #1
0.0416	0.0433	Top skin Spar #1 to Rear Spar
0.0416	0.0433	Top skin Rear Spar to Trailing edge
0.0416	0.0433	Bottom skin F/S to Spar #1
0.0416	0.0433	Bottom skin Spar #1 to Rear Spar
0.2079	0.2079	Top skin Rear Spar flange region
0.2079	0.2079	Bottom skin Rear Spar flange region
0.0416	0.0433	Bottom skin Rear Spar to Trailing edge
0.2772	0.2858	F/Spar (between H5 & H4 only)
0.1109	0.1126	F/Spar (except between H5 & H4)
0.1109	0.1039	Spar # 1
0.0832	0.0779	Rear Spar
0.1247	0.1300	Trailing edge (top & bottom skin joined together)
0.1109	0.1039	Actuator rib
0.0831	0.0779	Remaining ribs
0.0693	0.0693	Ibd/Obd rib
0.0831	0.0866	Top skin cut out region
0.0831	0.0866	Bottom skin cut out region
0.0554	0.0520	Top & Bottom skin between inbd rib &

Table 4: Results Matrix

New Material		Original Material
Eigenvalue at LL	1.036	0.995
Maximum Slope at LL (Aerodynamic Smoothness Requirements)	0.0195	0.0158
Maximum Tip Displacement (inches)	2.058	2.28
Weight Composites (lbs.)	30.33	35.73

VI. CONCLUSION

This paper addresses the use of a recently created design optimization methodology for an aircraft aileron. The work undertaken proves that even when structures are largely constrained, significant gains can be achieved by optimizing internal layouts of structural components. The 1st Eigenvalue was increased by approximately 23 % while the weight of the composite structure was reduced by 20%. Furthermore, the structural internal configuration derived should significantly reduce the manufacturing costs of the composite torsion box.

The productivity enhancements allowed by this tool can be increased further by the customization of certain parts of the analysis and the post-processing of the results. To this end and as part of the START Grant work, S. Rajbhandariet. al. (Reference 6) have developed GUI interfaces to allow for automatic assessment of aerodynamic smoothness and for the calculation of user defined failure criteria for composite materials and it's post-processing.

The methodology here described has been successfully employed in a number of control surfaces such as spoilers, rudders and flaps. The customization and standardization of these activities is currently being pursued for future projects.

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